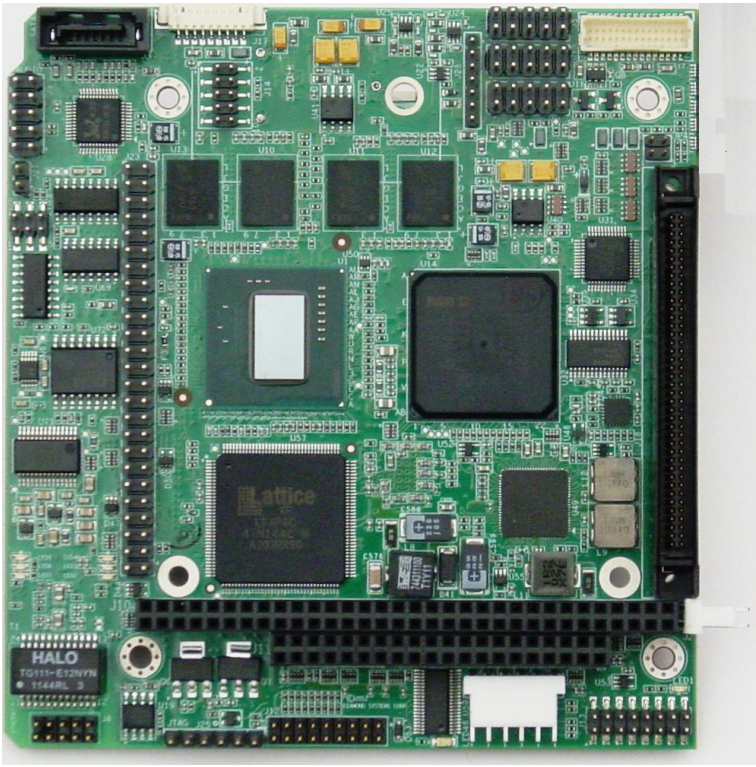
Athena III User Manual

High Integration PC/104 SBC with Gigabit Ethernet and Data Acquisition

Rev A.04: August 2015



Revision	Date	Comment
A.03	5/16/2014	Minor version
A.04	8/14/15	Temperature spec changed to +80°C

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1. IMPORTANT SAFE HANDLING INFORMATION

WARNING!

ESD-Sensitive Electronic Equipment

Observe ESD-safe handling procedures when working with this product.

Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.

Always store this product in ESD-protective packaging when not in use.

Safe Handling Precautions

The Helios board contains a high number of I/O connectors with connection to sensitive electronic components. This creates many opportunities for accidental damage during handling, installation and connection to other equipment. The list here describes common causes of failure found on boards returned to Diamond Systems for repair. This information is provided as a source of advice to help you prevent damaging your Diamond (or any vendor's) embedded computer boards.

ESD damage – This type of damage is usually almost impossible to detect, because there is no visual sign of failure or damage. The symptom is that the board eventually simply stops working, because some component becomes defective. Usually the failure can be identified and the chip can be replaced.

To prevent ESD damage, always follow proper ESD-prevention practices when handling computer boards.

Damage during handling or storage – On some boards we have noticed physical damage from mishandling. A common observation is that a screwdriver slipped while installing the board, causing a gouge in the PCB surface and cutting signal traces or damaging components.

Another common observation is damaged board corners, indicating the board was dropped. This may or may not cause damage to the circuitry, depending on what is near the corner. Most of our boards are designed with at least 25 mils clearance between the board edge and any component pad, and ground / power planes are at least 20 mils from the edge to avoid possible shorting from this type of damage. However these design rules are not sufficient to prevent damage in all situations.

A third cause of failure is when a metal screwdriver tip slips, or a screw drops onto the board while it is powered on, causing a short between a power pin and a signal pin on a component. This can cause overvoltage / power supply problems described below. To avoid this type of failure, only perform assembly operations when the system is powered off.

Sometimes boards are stored in racks with slots that grip the edge of the board. This is a common practice for board manufacturers. However our boards are generally very dense, and if the board has components very close to the board edge, they can be damaged or even knocked off the board when the board tilts back in the rack. Diamond recommends that all our boards be stored only in individual ESD-safe packaging. If multiple boards are stored together, they should be contained in bins with dividers between boards. Do not pile boards on top of each other or cram too many boards into a small location. This can cause damage to connector pins or fragile components.

Power supply wired backwards – Our power supplies and boards are not designed to withstand a reverse power supply connection. This will destroy each IC that is connected to the power supply (i.e. almost all ICs). In this case, the board will most likely cannot be repaired and must be replaced. A chip destroyed by reverse power or by excessive power will often have a visible hole on the top or show some deformation on the top surface due to vaporization inside the package. Check twice before applying power!

Board not installed properly in PC/104 stack – A common error is to install a PC/104 board accidentally shifted by 1 row or 1 column. If the board is installed incorrectly, it is possible for power and ground signals on the bus to make contact with the wrong pins on the board, which can damage the board. For example, this can damage components attached to the data bus, because it puts the ±12V power supply lines directly on data bus lines.

Overvoltage on analog input – If a voltage applied to an analog input exceeds the design specification of the board, the input multiplexor and/or parts behind it can be damaged. Most of our boards will withstand an erroneous connection of up to ±35V on the analog inputs, even when the board is powered off, but not all boards, and not in all conditions.

Overvoltage on analog output – If an analog output is accidentally connected to another output signal or a power supply voltage, the output can be damaged. On most of our boards, a short circuit to ground on an analog output will not cause trouble.

Overvoltage on digital I/O line – If a digital I/O signal is connected to a voltage above the maximum specified voltage, the digital circuitry can be damaged. On most of our boards the acceptable range of voltages connected to digital I/O signals is 0-5V, and they can withstand about 0.5V beyond that (-0.5 to 5.5V) before being damaged. However logic signals at 12V and even 24V are common, and if one of these is connected to a 5V logic chip, the chip will be damaged, and the damage could even extend past that chip to others in the circuit.

Bent connector pins – This type of problem is often only a cosmetic issue and is easily fixed by bending the pins back to their proper shape one at a time with needle-nose pliers. The most common cause of bent connector pins is when a PC/104 board is pulled off the stack by rocking it back and forth left to right, from one end of the connector to the other. As the board is rocked back and forth it pulls out suddenly, and the pins at the end get bent significantly. The same situation can occur when pulling a ribbon cable off of a pin header. If the pins are bent too severely, bending them back can cause them to weaken unacceptably or even break, and the connector must be replaced.

2. INTRODUCTION

Athena III is an embedded single-board computer (SBC) in a custom PC/104 small form factor that integrates a complete embedded PC and data acquisition circuitry into a single board.

The Athena III SBC is based on an Intel E-Series CPU with onboard central processing, memory and memory management devices and I/O management for specific functions. The board is larger than the PC/104 PCB format on three sides but uses the PC/104 mounting method and interface specification. The Athena III SBC includes the following additional features.

- Communicates externally over the ISA bus and I/O ports
- Generates on-board RGB video for CRT display systems
- Contains LVDS formatting to drive a flat panel
- Is powered from an externally regulated +5VDC supply

Four standard models of Athena III are available as shown in the following table.

Model	*Processor Speed*	*RAM Size*	*Data Acquisition*
ATHE1000A-1G	1GHz	1GB	Yes
ATHE1000D-1G	1GHz	1GB	DIO only
ATHE1600A-1G	1.6GHz	1GB	Yes
ATHE1600D-1G	1.6GHz	1GB	DIO only

The Athena III SBC uses the ISA bus, internally, to connect serial ports 1 through 4 and the data acquisition circuit to the processor. The ISA bus is brought out to an expansion connector to mate with add-on boards. Diamond Systems manufactures a wide variety of compatible PC/104 add-on boards for analog I/O, digital I/O, counter/timer functions, serial ports and power supplies.

Description and Features

The Athena III single board computer includes the following key system and data acquisition features.

2.1 Functions

The functions listed below are applicable for all models.

- Intel Atom E6xxT “Tunnel Creek” processors (Queensbay platform), clocked at 1.0GHz or 1.6GHz
- 1GB soldered DDR2 DRAM on 8 devices (533 or higher speed)
- 1 Gigabit Ethernet port on pin header, with on-board magnetics
- 4 USB 2.0 ports on headers
- 4 serial ports, all with RS-232/422/485 capability. COM1/COM2 and COM3/COM4 are always set to the same protocol in pairs. Individual protocol selection for each port is not available.
- USB flashdisk mounting location
- USB client
- LVDS flat panel interface up to 1280 x 768 maximum resolution
- VGA interface up to 1600 x 1200 maximum resolution
- 1 SATA port
- 24 digital I/O lines (provided by LPC-ISA FPGA)
- Programmable blue LED on board to indicate system status

2.2 Data Acquisition

The functions listed below are applicable to the DAQ version only.

- 16 channel single ended, 8 channel differential, 16-bit A/D
- 200KHz maximum sample rate
- Programmable input ranges +/-10V, +/-5V, +/-2.5V, +/-1.25V, 0-10V, 0-5V, 0-2.5V
- Interrupt-based sampling with 2048-sample programmable FIFO
- 4 12-bit D/A channels
- Jumper-selectable output ranges: +/-10V, +/-5V, 0-10V, 0-5V
- 24 digital I/O in 3 8-bit ports with programmable direction and buffered outputs
- 1 32-bit and 1 16-bit counter/timer for A/D sample rate control, event counting, and programmable interrupts
- Auto-calibration with Universal Driver software support for all data acquisition functions

2.3 Expansion Options

- USB flash-disk mounting capability up to 8GB
- PC/104 expansion connector

2.4 Operating System Support

- Windows Embedded Standard 7
- Linux 2.6
- Windows CE 6

2.5 Mechanical, Electrical, Environmental

- Expanded PC/104 form factor, 4.125”W x 4.475”H with custom corners, identical to Athena II
- Fanless heat sink on top side
- -40°C to +80°C ambient operating temperature without a fan
- MIL-STD-202G compatible
- Power input requirements: +5VDC +/- 5%
- Optional +12VDC to pass through to expansion buses and LCD backlight ONLY. No on-board circuits depend on +12VDC.

3. GETTING STARTED

First-time Athena III SBC users normally receive the product as part of Diamond's Athena III Development Kit, which provides everything needed to ensure rapid application development. This section of the Athena III User Manual covers basic hardware setup, power connection, system boot-up, and initial software configuration. After Athena III is up and running, refer to the later sections of this manual for the detailed hardware and software reference information needed to adapt the product to specific applications.

Important Safe-Handling Information

WARNING: ESD-Sensitive Electronic Equipment!

Observe ESD-safe handling procedures when working with this product.

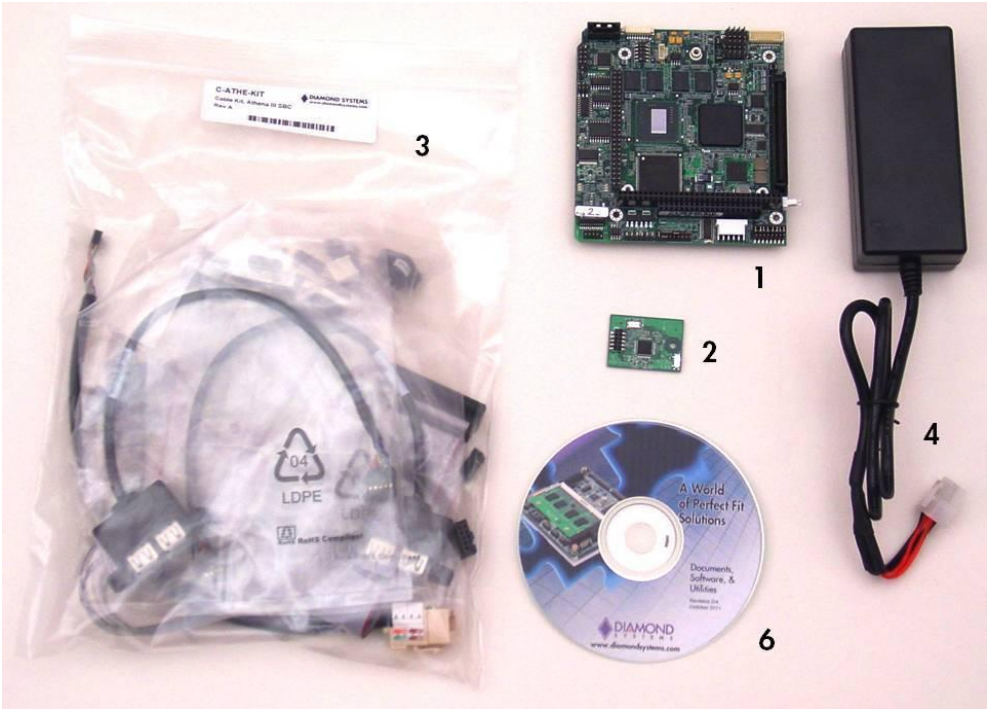
Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.

Always store this product in ESD-protective packaging when not in use.

Please refer to page 5 of this manual ("Important Safe-Handling Information") for further details.

3.1 Introducing the Athena III Development Kit

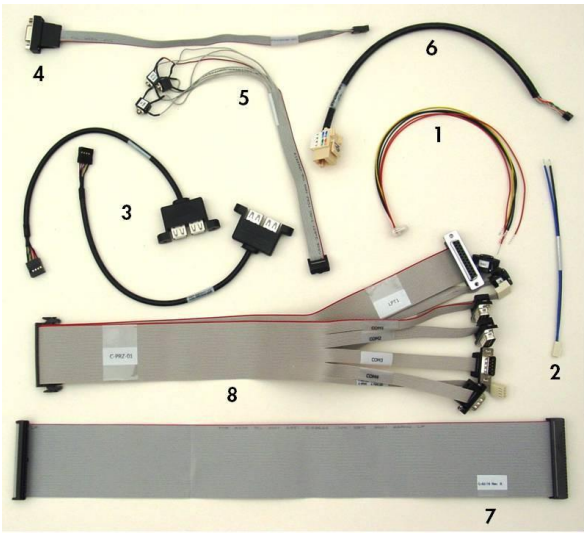
The Athena III Development Kit (for example DK-ATHE-A-LNX for the Linux version) provides everything required for Athena III based rapid application development. The table on the next page lists the boards, cables, and other items included.



Item	Diamond P/N	Description
1	ATHE1600A-1G	Athena III SBC, 1.6GHz Atom E640T CPU, 1GB SDRAM, Data Acquisition
2	8890653	8GB USB flashdisk with bootable Linux pre-loaded
3	C-ATHE-KIT	Athena III Cable Kit
4	PS-5V-04	5V AC Power Adapter
5	7460651	Athena III Quick Start Guide (not shown)
6	6710010	Diamond Systems Software and Documentation CD
7	DOC-PKG	Diamond Systems Document Package (not shown)
8	MTG104	PC/104 Mounting Hardware Kit (not shown)

3.1.1 Athena III Cable Kit

The Athena III Cable Kit (number C-ATHE-KIT) provides convenient access to most of Athena III's I/O features. The kit's cable assemblies are shown in the photo below, and identified in the table that follows.



Item	Qty	Description	Diamond P/N	Connects to…
1	1	Power input cable	6981506	J21
2	1	External battery cable	6981011	J2
3	2	Dual USB cable	6981012	J15 and J16
4	1	VGA cable	6981030	J5
5	1	Audio cable	6981031	J9
6	1	Gigabit Ethernet cable	6981080	J4
7	1	Data Acquisition cable	C-50-18	J23
8	1	Main I/O cable	C-PRZ-01	J18

Note: *On each interface cable, the end of the cable connector that has a red wire going to it should be oriented toward the end of the board connector that is labeled "pin 1" (typically the pin with a square pad on the PCB).*

3.2 System Setup

This section outlines a simple process for preparing Athena III for first-time operation using the Athena III Development Kit. Additional details regarding Athena III's interface functions and connections may be found in Section 6 of this document (Connectors).

3.2.1 Unpacking

Unpack and remove the Athena III single board computer from its packaging.

3.2.2 Mounting Kit

Install the four standoffs found in the mounting kit (MTG104) into the four PC/104 mounting holes located at each corner of the board on the bottom side of the SBC. This ensures that the SBC will not touch the surface beneath it, and helps redistribute the force when you push connectors onto the board.

3.2.3 Keyboard and Mouse

Athena III supports operation using a PS/2-based keyboard and mouse devices. Plug the keyboard and mouse connectors into the appropriate connectors on the Main I/O cable in the Athena III Cable Kit (cable number C-PRZ-01). Connect the end of the cable into connector J18 on Athena III.

3.2.4 USB Flashdisk Socket

Athena III provides a location for on-board installation of an optional USB flashdisk on connector J14. Plug the USB flashdisk module in the Development Kit into connector J14 on Athena III. Remove the screw from the mounting stand-off before installing the flashdisk. Secure the flashdisk to Athena III with the screw once the flashdisk is installed.

3.2.5 Mass Storage Devices

If desired, connect SATA hard drives to Athena III by connecting a SATA cable to SATA connector J3 and then to the SATA drive. Athena III can operate with a combination of SATA and CD-ROM drives, and can boot from either of them.

> ***Caution!*** *Be sure the* PS-5V-04 *AC power adapter is disconnected from its AC power source prior to performing the following step.*

3.2.6 Connecting Power

Connect cable 6981506 to the PS-5V-04 AC power adapter or an ATX power supply. Connect the other end of the 6981506 cable to connector J21 on the Athena III SBC.

3.2.7 Display

Athena III provides interfaces for both LVDS flat panel displays and VGA output. Connect the VGA cable, 6981030, between the VGA connector, J5, and a VGA-compatible display.

3.3 Booting the System

Power-up the VGA video monitor. Then plug the PS-5V-04 AC power adapter to an AC outlet. Athena III should begin its boot-up sequence immediately, as evidenced by BIOS messages on the connected VGA display. You can run the BIOS Setup utility and proceed to install an operating system on the boot drive just as you would on a normal desktop PC.

3.3.1 BIOS Setup

Athena III's BIOS provides a wide range of configuration options. When you power up Athena III for the first time, you should immediately enter the BIOS "Setup" utility in order to adjust BIOS settings to match your system's peripheral devices and other requirements, and to configure various other hardware and software parameters.

Options configurable via Setup typically include:

- Number and type of mass storage devices
- Boot device priority
- Video display type and resolution
- IDA, SATA, serial, and parallel interface modes and protocols
- PCI and PnP configuration
- Power management setup
- Automatic power-up after LAN connection, RTC alarm, power resumption, etc.
- System monitoring and security functions

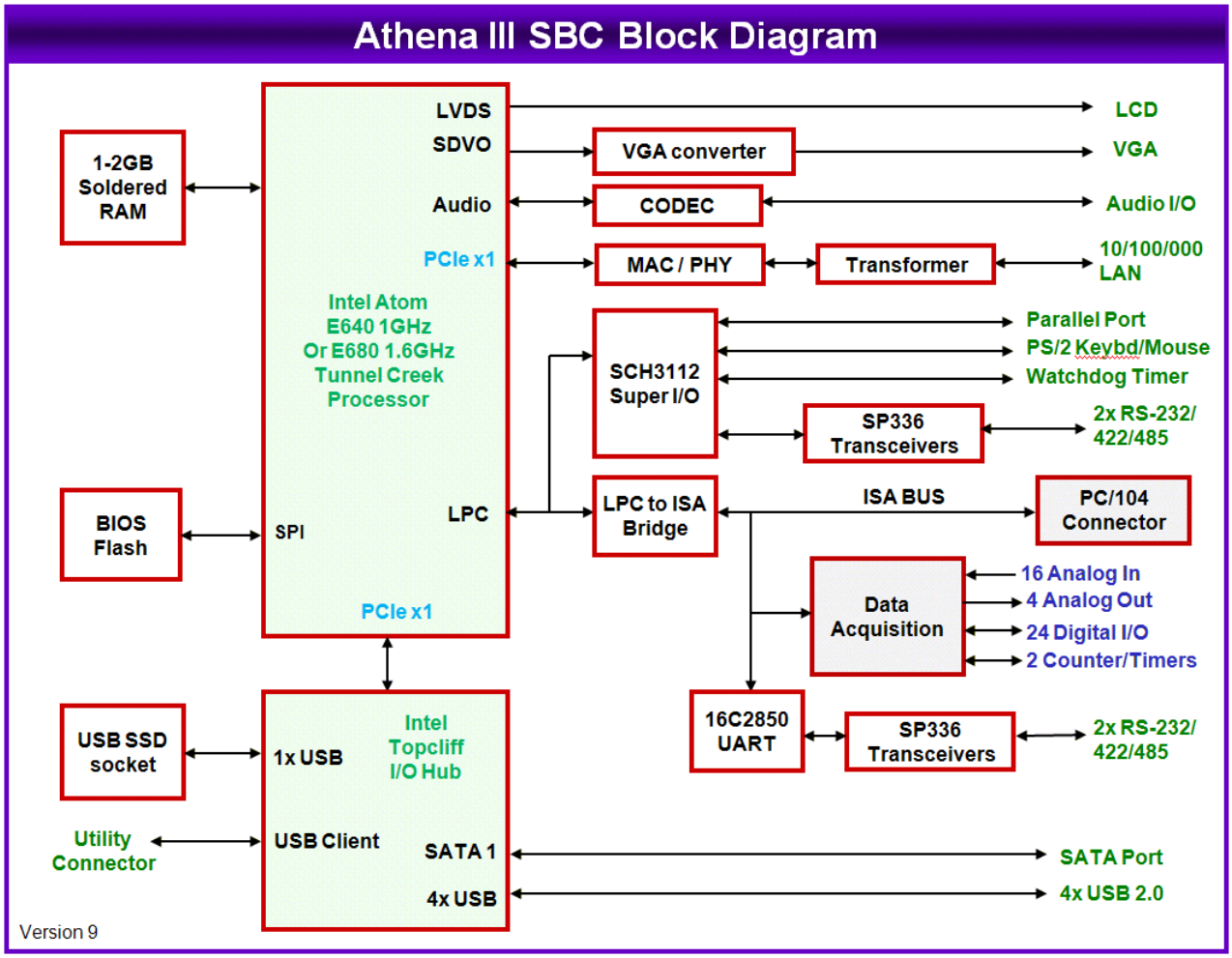
3.3.2 Operating System Drivers

Athena III will boot and run a Linux 2.6 operating system from the USB flashdisk. Athena III should now be fully operational.

If you desire to run a different operating system, depending on the operating system to be installed, it may be necessary to install software drivers for on-board interface controllers. Drivers for Windows Embedded Standard 7, Windows Embedded CE, and Linux 2.6, if required, are included on the Software and Documentation CD that is included in the Athena III Development Kit.

4. FUNCTIONAL OVERVIEW

4.1 Functional Block Diagram



4.2 Functional Overview

This section describes the major Athena III subsystems.

4.2.1 CPU Core

Athena III's core embedded computer circuit features the ultra low power Intel Atom "Queensbay" extended temperature platform, consisting of an Atom processor ("Tunnel Creek") with I/O Hub ("Topcliff"). The rest of the circuit consists of 1GB of soldered DRAM memory using 8 chips, a display controller with LVDS and onboard VGA/ DVI converter, plus SATA, USB, serial port and LAN interfaces. The ISA is available for stackable I/O expansion.

4.2.2 Video

LVDS and SDVO from the chipset are provided on I/O connectors. LCD power may be jumper-selected for +3.3VDC or +5VDC. Backlight power may be jumper-selected for +5VDC or +12VDC. The +12VDC is routed from the input power connector and is only available if supplied by the customer; it is not generated on board.

An SDVO to VGA converter circuit is provided on the board to offer video display directly on-board. There is only one SDVO channel available.

4.2.3 Ethernet

Athena III provides a Gigabit Ethernet port derived from an Intel 82574ITMAC/PHY connected via PCIe from Tunnel Creek. A gigabit magnetic chip and header complete the circuit.

4.2.4 USB

Athena III offers five user accessible USB 2.0 ports. All ports have minimum 500mA per port drive capability with short circuit / over current and ESD protection on each port. Ports 1-4 are brought out to I/O connectors for user access, and port 5 is used for a board-mountable USB flashdisk. One USB client port will be available via a utility connector.

4.2.5 USB Solid State Storage

A separate USB connector is provided for mounting a solid state bootable USB flashdisk module with capacity up to 8GB.

4.2.6 Serial Ports

Athena III provides four serial ports with varying protocols and signal availability. The SCH3114 provides two of the serial ports. The other two serial ports are derived from the 16C2850 UART and provide 128 byte transmit / receive buffers. To maintain Athena II compatibility the 16C2950 ports are assigned to COM3, COM4. The BIOS supports serial console on COM ports 1 or 2.

4.2.7 Data Acquisition

The SBC provides the following data acquisition capabilities.

Type of I/O	***Characteristics***
Analog Input	16 single-ended/8 differential inputs, 16-bit resolution 200KHz maximum aggregate A/D sampling rate Programmable input ranges/gains: +/-10V, +/-5V, +/-2.5V, +/-1.25V, 0-10V, 0-5V, 0-2.5V A/D FIFO for reliable high-speed sampling and scan operation
Analog Output	Four analog outputs, 12-bit resolution ±10V, +/-5V, 0-10V, and 0-5V output ranges Indefinite short circuit protection on outputs
Digital I/O	24 programmable digital I/O, 3.3V and 5V logic compatible
Counter/Timers	One 32-bit counter/timer for A/D sampling rate control One 16-bit counter/timer for user counting and timing functions

On board I^2C flash EEROM is provided for auto-calibration value storage.

4.2.8 PC/104 Expansion Bus

The PC/104 expansion bus enables installation of additional I/O boards. It consists of two stack-through connectors press-fit onto the board, enabling expansion both above and below the board.

4.2.9 Power Supply

Athena III runs on a fixed input of +5 VDC +/-5%. In addition, a pin is available for users to attach +12VDC; however this voltage is routed only to the LCD backlight connector and the PC/104 expansion bus connectors. No on-board circuit connects to +12V. Every circuit connects to +5V or to supplies derived from +5V.

4.2.10 Watchdog Timer

A programmable watchdog timer (WDT) is included to provide an automatic reset in case of system hang. The WDT may be retriggered either by a software command or a digital input. The system will reset when the WDT is enabled and expires.

The WDT circuitry is integrated into the SCH31121 SIO chip.

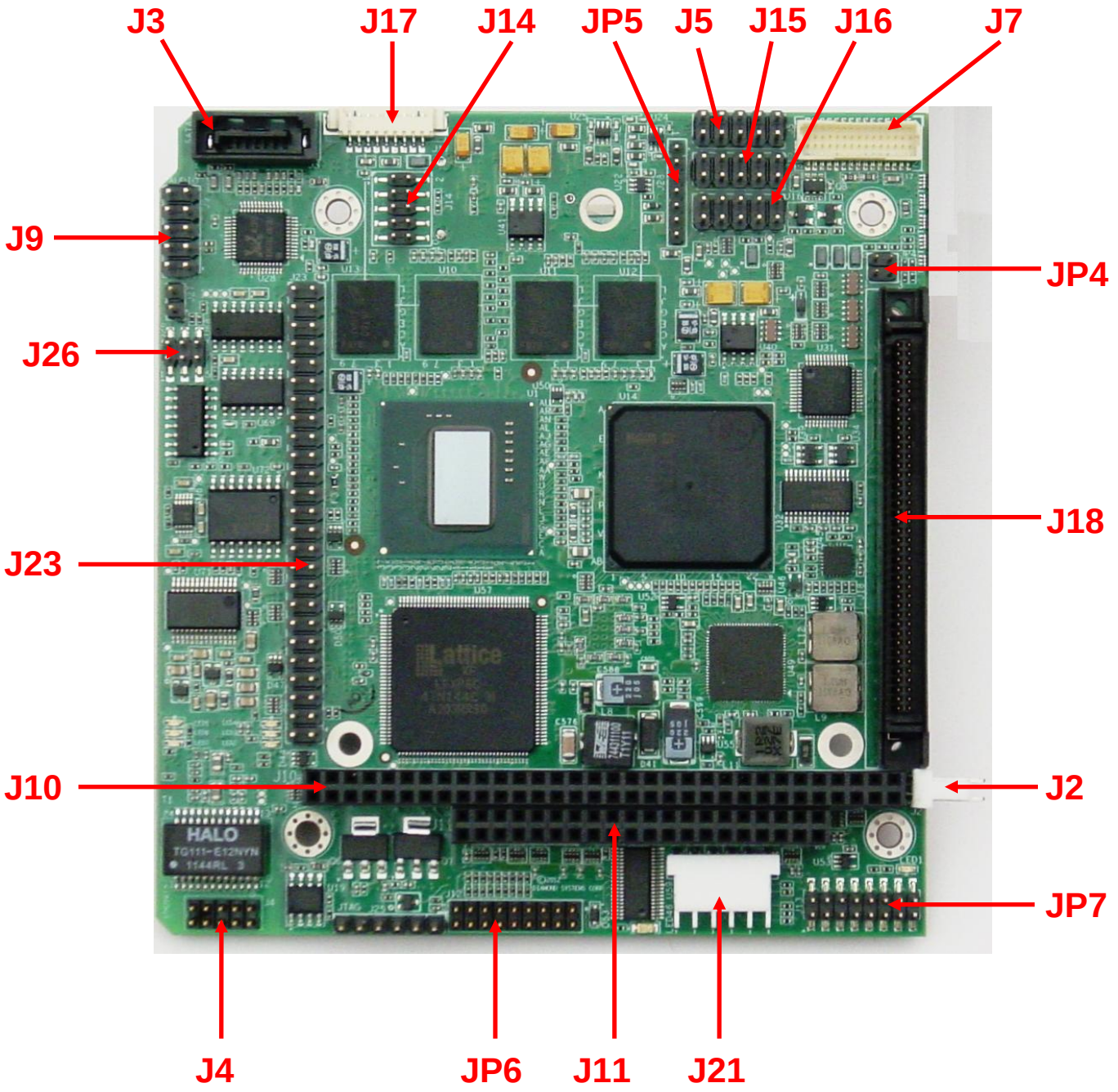
4.2.11 BIOS

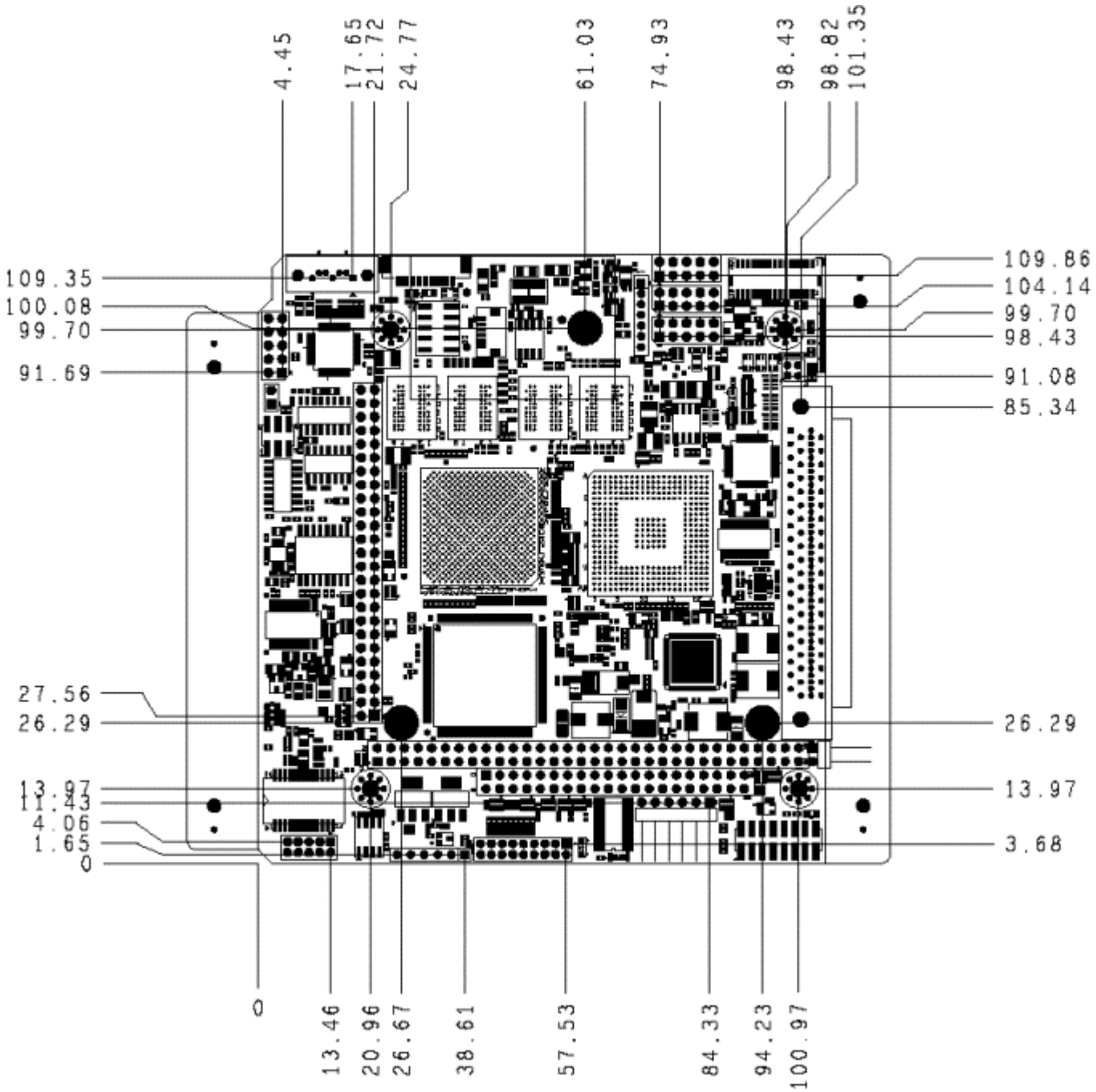
The AMI BIOS includes the following key features:

- Boot from LAN (PXE) and USB as well as C: and D:
- User selectable Master boot device selection
- Free boot sequence configuration
- Support for various LCD configurations supported by the video chipset
- Console (display and keyboard) redirection to serial port
- BIOS recovery through USB attached storage or other means
- Configurable default settings in battery-less configurations
- Initialize USB keyboard & mouse
- Customizable splash screen

5. BOARD DESCRIPTION

The figure below shows the Athena III SBC layout with connector and jumper block locations labeled. On the following page is a figure showing the key dimensions on the Athena III PCB in millimeters.

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61.03
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13.97
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4.06
1.65
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13.97
3.68
0
13.46
20.96
26.67
38.61
57.53
84.33
94.23
100.97

5.1 Connector Summary

The following table lists the connectors on the Athena III SBC.

Connector	*Description*
J2	External Battery
J3	SATA
J4	Ethernet
J5	VGA
J7	LVDS LCD
J8	LCD Backlight Power (on bottom of SBC)
J9	Audio I/O
J10	PC/104, ISA bus A,B
J11	PC/104, ISA bus C,D
J14	USB flashdisk
J15	USB 0/1
J16	USB 2/3
J17	USB Client Port & Utility
J18	Main I/O (serial ports, PS/2 keyboard/mouse, parallel port, utility)
J21	Input Power
J23	Data Acquisition I/O

5.2 Jumper Summary

The following table lists the jumpers on the Athena III SBC.

Jumper Block	*Description*
JP4	LCD scan direction and frame rate setting
JP5	LCD panel voltage select
JP6	System configuration settings
JP7	RS-232/422/485 termination select
J26	Data acquisition configuration settings

5.3 LED Summary

The following table lists the LEDs found on the Athena III SBC.

LED Number	*Description*	*Color*
LED46	DAQ/FPGA loaded successfully	Blue
LED1	SATA activity	Green
LED2	Ethernet activity	Green
LED3	Ethernet Link 100Mbps	Green
LED4	Ethernet Link 1000Mbps	Yellow
LED5	Power +5V	Green
LED6	Power +3.3V	Green
LED7	Power +3.3V switched, S4/S5	Yellow

6. CONNECTORS

This section describes the on-board Athena III connectors.

> **Note:** All cables mentioned in this chapter are included in Diamond Systems' cable kit C-ATHE-KIT. Some cables are also available individually.

6.1 External Battery (J2)

Connector J2 is used to connect an external battery for maintaining the Real-Time Clock and the CMOS settings (BIOS settings for various system configurations). The battery voltage for this input should be 3-3.6VDC. The current draw averages under 4µA at 3V.

J2 External Battery Connector (end view)

1	Battery input (+)
2	Ground

Connector on board: Tyco 640457-2 right-angle friction lock pin header or equivalent

6.2 SATA (J3)

The SATA connector is an industry-standard vertical connector.

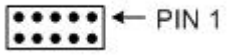
1	Ground
2	Transmit+
3	Transmit-
4	Ground
5	Receive-
6	Receive+
7	Ground

Connector type: SAMTEC

6.3 Ethernet (J4)

Athena III provides one Gigabit Ethernet port. The I/O connector pinout is designed so that the left column matches the 10/100 Ethernet pinout on Athena II for backward compatibility with existing Athena II mating cables and applications. For Gigabit operation all 10 pins are used.

J4 Ethernet Connector (end view)



NC	1	2	Key / Cut
DA+	3	4	DA-
DB+	5	6	DB-
DC+	7	8	DC-
DD+	9	10	DD-

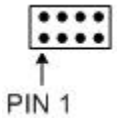
Connector type: Standard 2mm dual row straight pin header with gold flash plating

Connector on board: Molex 87758-1016 or equivalent

6.4 VGA (J5)

Connector J5 is a 2x4-pin header for connecting a VGA monitor.

J5 VGA Connector (end view)



Green	1	2	Red
Blue	3	4	Ground
HSYNCE	5	6	DDC data
VSYNC	7	8	DDC clock

Signal	***Definition***
Ground	Ground return
Red	RED signal (positive, 0.7Vpp into 75 Ohm load)
Green	GREEN signal (positive, 0.7Vpp into 75 Ohm load)
Blue	BLUE signal (positive, 0.7Vpp into 75 Ohm load)
DDC clock/data	Digital serial I/O signals used for monitor detection (DDC1 specification)
HSYNC	Horizontal sync
VSYNC	Vertical sync

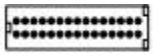
Note: While the DDC serial detection pins are present, a 5V power supply is not provided (the old "Monitor ID" pins are also not used).

Diamond Systems cable number 6981030 provides a female DB15 connection to interface with a standard RGB monitor.

6.5 LCD Panel, LVDS Interface (J7)

Connector J7 provides access to the internal LVDS LCD display drivers. See below for connector J8 for LCD backlight information. The LCD panel power is jumper-selectable for 3.3V (default) or 5V. The Intel Atom E-Series CPU has maximum allowable LCD support of 1280 x 768.

J7 LCD Panel Connector (end view)



Ground	1	2	Ground
LVDS clock-	3	4	
LVDS clock+	5	6	
Ground	7	8	Ground
LVDS data 0-	9	10	LVDS data 3+
LVDS data 0+	11	12	LVDS data 3-
Ground	13	14	Ground
LVDS data 2-	15	16	
LVDS data 2+	17	18	
Ground	19	20	Ground
LVDS data 1+	21	22	Scan Direction
LVDS data 1-	23	24	LVDS Map
Ground	25	26	Ground
VDD (LCD display)	27	28	VDD (LCD display)
VDD (LCD display)	29	30	VDD (LCD display)

Signal	***Definition***
LVDS Data 0-2 +/-	Primary Data Channel, bits 0-2 (LVDS Differential signaling)
LVDS Clock +/-	Primary Data Channel, Clock (LVDS Differential signaling)
LVDS Data 0-2 +/-	Secondary Data Channel, bits 0-2 (LVDS Differential signaling)
LVDS Clock +/-	Secondary Data Channel, Clock (LVDS Differential signaling)
VDD	+3.3V Switched Power Supply for LCD display (only powered up when LCD display is active)
Ground	Power Ground, 0V

Connector on board: JST model number BM30B-SRDS-G-TF or equivalent

Mating cable connector: JST model number SHDR-30V-S-B or equivalent
Terminals: JST model number SSH-003GA-P0.2 or equivalent

6.6 LCD Backlight (J8)

Connector J8 provides the backlight power and control for the optional LCD panel. See the description for connector J7, above, for details on the LCD data interface.

J8 LCD Backlight Connector (end view)

1	Power +5V/+12v, jumper selectable
2	Power (same as pin 1)
3	Ground
4	Ground
5	Enable (GPIO output), 0 = off, open circuit = on
6	Brightness, 0-5VDC variable; 0V = max, 5V = min

The brightness control for the LCD backlight has a weak pull-down resistor to ensure maximum brightness when it is not connected externally. Brightness may be controlled by a GPIO pin on the CPU or embedded microcontroller or by pin 6 on this connector. A jumper selects the source of the brightness signal to this pin.

Connector on board: Molex 53047-0610 or equivalent

Mating Cable Connector: Molex 51021-0600 or equivalent

Terminals: Molex 50058 / 50079 series or equivalent

6.7 Audio (J9)

Connector J9 provides the audio signals.

Line Out Left	1	2	Line Out Right
Ground	3	4	Line In left
Lin In Right	5	6	Ground
MIC In	7	8	NC
NC	9	10	Ground

Connector type: Standard 0.1” dual row straight pin headers with gold flash plating

6.8 PC/104 ISA Bus (J10, J11)

Connectors J10 and J11 carry the ISA bus signals. The following diagram shows the PC/104 A and B pin layout for J10 and the C and D pin layout for J11.

J10

IOCHCHK-	A1	B1	Ground
SD7	A2	B2	RESETDRV
SD6	A3	B3	+5V
SD5	A4	B4	IRQ9
SD4	A5	B5	-5V
SD3	A6	B6	DRQ2
SD2	A7	B7	-12V
SD1	A8	B8	ENDXFR-
SD0	A9	B9	+12V
IOCHRDY	A10	B10	Key
AEN	A11	B11	SMEMW-
SA19	A12	B12	SMEMR-
SA18	A13	B13	IOW-
SA17	A14	B14	IOR-
SA16	A15	B15	DACK3-
SA15	A16	B16	DRQ3
SA14	A17	B17	DACK1-
SA13	A18	B18	DRQ1
SA12	A19	B19	REFRESH-
SA11	A20	B20	SYSCLK
SA10	A21	B21	IRQ7
SA9	A22	B22	IRQ6
SA8	A23	B23	IRQ5
SA7	A24	B24	IRQ4
SA6	A25	B25	IRQ3
SA5	A26	B26	DACK2-
SA4	A27	B27	TC
SA3	A28	B28	BALE
SA2	A29	B29	+5V
SA1	A30	B30	OSC
SA0	A31	B31	Ground
Ground	A32	B32	Ground

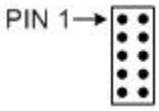
J11

Ground	C0	D0	Ground
SBHE-	C1	D1	MEMCS16--
LA23	C2	D2	IOCS16-
LA22	C3	D3	IRQ10
LA21	C4	D4	IRQ11
LA20	C5	D5	IRQ12
LA19	C6	D6	IRQ15
LA18	C7	D7	IRQ14
LA17	C8	D8	DACK0-
MEMR-	C9	D9	DRQ0
MEMW-	C10	D10	DACK5-
SD8	C11	D11	DRQ5
SD9	C12	D12	DACK6-
SD10	C13	D13	DRQ6
SD11	C14	D14	DACK7-
SD12	C15	D15	DRQ7
SD13	C16	D16	+5
SD14	C17	D17	MASTER-
SD15	C18	D18	Ground
Key	C19	D19	Ground

6.9 USB Flashdisk (J14)

This connector is used for the USB flash memory interface. This is a dedicated USB port.

J14 USB Connector (end view)



USB Pwr-	1	2	NC
USB Data-	3	4	NC
USB Data+	5	6	NC
Ground	7	8	NC
Key	9	10	NC

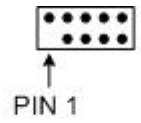
Connector type: 2mm dual row SMD straight 10 POS

Connector on board: Sullins NRPN052MASMS-RC or equivalent

6.10 USB (J15, J16)

Connectors J15 (USB 0/1) and J16 (USB 2/3) provide four USB 2.0 ports. The connectors have identical pinouts as described below.

J15/J16 USB Connectors



Key (pin cut)	1	2	Shield
GND	3	4	GND
USB1/3 D+	5	6	USB0/2 D+
USB1/3 D-	7	8	USB0/2 D-
USB1/3 VCC	9	10	USB0/2 VCC

Signal	*Definition*
VCC	+5VDC
D-	Data +
D+	Data -
GND	Ground

Connectors J15 and J16 mate with Diamond Systems cable number 698012, which provides two standard USB type A jacks in a panel-mount housing.

Connector type: Standard 0.1” dual row straight pin headers with gold flash plating

6.11 Main I/O (J18)

An 80-pin high-density connector is provided for access to legacy I/O plus miscellaneous functions. The following functions are supported by this connector.

- Four serial ports
- Parallel port
- PS/2 keyboard
- PS/2 mouse
- IDE port
- ATX Power switch
- Reset switch
- Power and HDD LEDs

J18 Main I/O Connector

COM1 – COM4 signals depend on the selected protocol. The pinout shown on the next page is for RS-232.

For RS-422 or RS-485, the following pinouts apply:

RS-422	1/10/19/28	NC
	2/11/20/29	NC
	3/12/21/30	TXD+
	4/13/22/31	TXD-
	5/14/23/32	Ground
	6/15/24/33	RXD-
	7/16/25/34	RXD+
	8/17/26/35	NC
	9/18/27/36	Ground

RS-485	1/10/19/28	NC
	2/11/20/29	NC
	3/12/21/30	NC
	4/13/22/31	TXD/RXD-
	5/14/23/32	TXD/RXD+
	6/15/24/33	NC
	7/16/25/34	NC
	8/17/26/35	NC
	9/18/27/36	Ground

Cable A			Cable B		
COM1	DCD1	1	1	STB-	*LPT1*
	DSR1	2	2	AFD-	
	RXD1	3	3	PD0	
	RTS1	4	4	ERR-	
	TXD1	5	5	PD1	
	CTS1	6	6	INIT-	
	DTR1	7	7	PD2	
	RI1	8	8	SLIN-	
	GND	9	9	PD3	
COM2	DCD2	10	10	GND	
	DSR2	11	11	PD4	
	RXD2	12	12	GND	
	RTS2	13	13	PD5	
	TXD2	14	14	GND	
	CTS2	15	15	PD6	
	DTR2	16	16	GND	
	RI2	17	17	PD7	
	GND	18	18	GND	
COM3	DCD3	19	19	ACK-	
	DSR3	20	20	GND	
	RXD3	21	21	BUSY	
	RTS3	22	22	GND	
	TXD3	23	23	PE	
	CTS3	24	24	GND	
	DTR3	25	25	SLCT	
	RI3	26	26	KB Clk	*KYBD*
	GND	27	27	KB/MS V-	
COM4	DCD4	28	28	KB Data	
	DSR4	29	29	KB/MS V+	
	RXD4	30	30	MS Clk	*Mouse*
	RTS4	31	31	KB/MS V-	
	TXD4	32	32	MS Data	
	CTS4	33	33	KB/MS V+	
	DTR4	34	34	GND	*Utilities B*
	RI4	35	35	Reset-	
	GND	36	36	Power	
Utilities A	+5V Out	37	37	NC	
	Speaker Out	38	38	NC	
	SATA Drive LED	39	39	NC	
	Power LED	40	40	NC	

Signal Group	*Signal*	*Description*
COM1-COM4	-	The signals on these pins are RS-232 level signals and may be connected directly to RS-232 devices. The pinout of these signals is designed to allow a 9-pin male IDC connector to be crimped onto the corresponding ribbon cable wires to provide the correct pinout for a PC serial port connector (DTE).
LPT1	-	The signals on these pins comprise a standard PC parallel port. The pinout of these signals is designed to allow a 25-pin female IDC connector to be crimped onto the corresponding ribbon cable wires to provide the correct pinout for a PC parallel port connector.
KYBD, Mouse	-	PS/2 signals for keyboard and mouse. (Pins 2 and 6 on the Mini-Din-6 PS/2 connectors are unused).
	KB Clk	Clock pin; connects to pin 5 of the PS/2 connector.
	KB/MS V-	Power pin; connects to pin 3 of the PS/2 connector.
	KB Data	Data pin; connects to pin 1 of the PS/2 connector.
	KB/MS V+	Power pin; connects to pin 4 of the PS/2 connector.
Utilities A	+5V Out	Switched power pin that is turned on and off with the ATX power switch or with the +5V input.
	Speaker Out	Referenced to +5V Out. Connect a speaker between this pin and +5V Out.
	SATA Drive LED	Referenced to +5V Out. Does not require a series resistor. Connect LED directly between this pin and +5V Out.
	Power LED	Referenced to +5V Out. Does not require a series resistor. Connect LED directly between this pin and +5V Out.
Utilities B	Reset-	Connection between this pin and Ground will generate a Reset condition.
	ATX Power	When ATX is enabled, a momentary contact between this pin and ground causes the CPU to turn on, and a contact of 4 seconds or longer will generate a power shutdown.

Connector J18 mates with Diamond Systems cable number C-PRZ-01, which consists of a dual-ribbon-cable assembly with industry-standard connectors at the user end. The SBC mating connector includes integral latches for enhanced reliability. Each ribbon cable has 40 wires.

Connector type: 3M P50E-080P1-S1-EA connector or equivalent

6.12 Input Power (J21)

Input power for Athena III may be supplied either from an external supply, through J21, or directly through the PC/104 bus power pins if a PC/104 power supply is used with the SBC.

1	+5V In
2	Ground
3	Ground
4	+12V In (optional)
5	Ground
6	+5V In

- Athena III requires only +5VDC input power to operate. All other required voltages are generated on board with miniature switching regulators. However since the PC/104 bus includes pins for ±5V and ±12V, these voltages may be supplied through J11 if needed. The +5V and +12V voltages are controlled by the ATX power manager switches, while -5V and -12V are routed directly to the corresponding pins on PC/104 bus and are not controlled by the ATX function.
- Make sure that the power supply used has enough current capacity to drive your system. The Athena III SBC requires up to 3A on the +5V line. If you have a disk drive or other modules connected, you need additional power. In particular, many disk drives need extra current during startup. If your system fails to boot properly, or if disk accesses do not work properly, the first thing to check is the power supply voltage level. Many boot-up problems are caused simply by insufficient voltage due to excess current draw on the +5V supply.
- Multiple +5V and Ground pins are provided for extra current carrying capacity if needed. Each pin is rated at 3A max (15W). For the Athena III SBC and panel I/O board 3A is sufficient, so +5V and Ground require only a single wire each. In this case the first 4 pins may be connected to a standard 4-pin miniature PC power connector if desired. Be advised that some voltage will be dropped in the wire depending on the wire gauge (AWG).
- For a larger PC/104 stack the total power requirements should be calculated to determine whether additional wires are necessary.
- ATX control enables the +5V and +12V power to be switched on and off with an external momentary switch. A short press on the switch will turn on power, and holding the switch on for 4 seconds or longer will turn off power.

Connector type: AMP/Tyco Friction Lock latching right-angle connector (TE Connectivity 3-641191-6)

Data Acquisition I/O (J23)

J23 Data Acquisition I/O Connector

Athena III includes a 50-pin header, J23, for all data acquisition I/O with the pin out below.

DIO A0	1	2	DIO A1
DIO A2	3	4	DIO A3
DIO A4	5	6	DIO A5
DIO A6	7	8	DIO A7
DIO B0	9	10	DIO B1
DIO B2	11	12	DIO B3
DIO B4	13	14	DIO B5
DIO B6	15	16	DIO B7
DIO C0	17	18	DIO C1
DIO C2	19	20	DIO C3
DIO C4/GATE0	21	22	DIO C5/GATE1
DIO C6/CLK1	23	24	DIO C7/OUT0
EXTTRIG	25	26	TOUT1
+5V out	27	28	DGND
VOUT0	29	30	VOUT1
VOUT2	31	32	VOUT3
AGND(Vout)	33	34	AGND(Vin)
VIN0	35	36	VIN8
VIN1	37	38	VIN9
VIN2	39	40	VIN10
VIN3	41	42	VIN11
VIN4	43	44	VIN12
VIN5	45	46	VIN13
VIN6	47	48	VIN14
VIN7	49	50	VIN15

Signal	*Definition*
DIO A7-A0	Digital I/O port A; programmable direction
DIO B7-B0	Digital I/O port B; programmable direction
DIO C7-C0	Digital I/O port C; programmable direction C7-C4 may be configured for counter/timer signals
EXTTRIG	External A/D trigger input
TOUT1	Counter/Timer 1 output
Vin 7/7+ ~ Vin 0/0+	Analog input channels 7 – 0 in single-ended mode High side of input channels 7 – 0 in differential mode
Vin 15/7- ~ Vin 8/0-	Analog input channels 15 – 8 in both single-ended mode Low side of input channels 7 – 0 in differential mode
VOUT0-3	Analog output channels 0 – 3
+5V out	Connected to switched +5V supply (Output only! Do not connect to external supply)
DGND	Digital ground (0V - reference); used for digital circuitry only
AGND	Analog ground; used for analog circuitry only Vout pin is for analog outputs, Vin pin is for analog inputs

Diamond Systems cable number C-50-18 provides a standard 50-pin connector at each end and mates with this header.

Connector type: Standard .1" single row straight pin header with gold flash plating

7. JUMPER CONFIGURATION

The Athena III SBC has the following jumper-selectable configuration options.

Jumper Block	*Description*
JP4	LCD scan direction and frame rate setting
JP5	LCD panel voltage select
JP6	System configuration settings
JP7	RS-232/422/485 termination select
J26	Data acquisition configuration settings

7.1 LCD Scan and Frame Rate Settings (JP4)

Jumper block JP4 is use to configure LCD scan and frame rate settings.

JP4 Jumper Block with Default Settings

7.2 LCD Panel Voltage Select (JP5)

Jumper block JP5 is use to select the LCD panel and backlight voltages. Only the four jumper locations described below are valid locations.

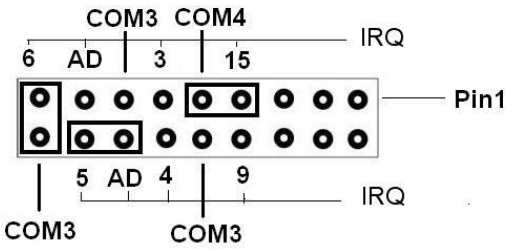
JP5 Jumper Block with Default Settings

Jumper Location	*Function*
Pins 1-2	LCD VDD set to +5V (default)
Pins 2-3	LCD VDD set to +3.3V
Pins 5-6	Backlight inverter VDD set to +5V (default)
Pins 6-7	Backlight inverter VDD set to +12V

7.3 System Configuration Settings (JP6)

Jumper block JP6 is used to configure IRQ levels.

JP6 Jumper Block with Default Settings



Pin Number	*Function*
7, 9	IRQ 15; selectable for COM4
14,16	IRQ 5; selectable for A/D IRQ
17,18	IRQ 6; selectable for COM3

COM3, COM4 and A/D IRQ settings can be configured as shown in the following table.

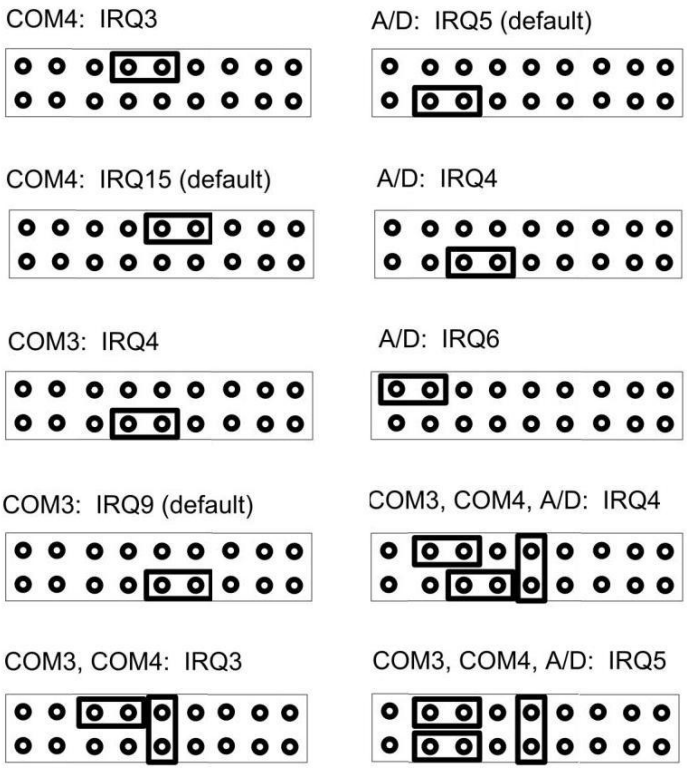
Device	*IRQ3*	*IRQ4*	*IRQ5*	*IRQ6*	*IRQ9*	*IRQ15*
COM3	X	X	X	X (default)	X	-
COM4	X	-	-	-	-	X (default)
A/D	-	X	X (default)	X	-	-

Note: IRQ4 can only be used for the data acquisition circuit if it is not already used for COM3.

It is possible to set up all three circuits to share either IRQ4 or IRQ5. However, only one device can use the shared IRQ at a time; the ability for all three devices to run simultaneously is not supported.

Configure the IRQ options as shown in the following jumper settings.

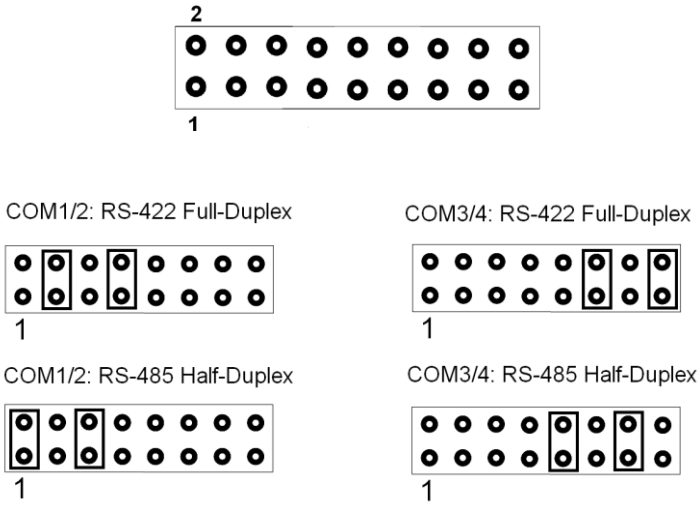
IRQ Configuration Options



7.4 RS-232/422/485 Termination Select (JP7)

Jumper block JP7 is used to configure RS-232/422/485 termination selection.

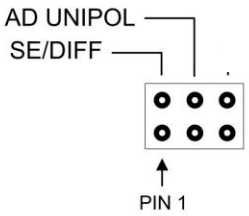
JP7 RS-232/422/485 Default Jumper Settings



7.5 Data Acquisition Configuration (J26)

Jumper block J26 is used to configure the A/D and D/A circuits

J26 Jumper Block



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Jumper Label	*Configuration Function*
SE/DIFF	A/D single-ended/differential selection.
AD UNIPOL	A/D unipolar/bipolar selection.

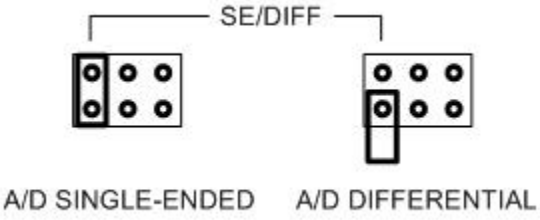
7.5.1 Single-Ended/Differential Input Settings

Athena III can accept both single-ended and differential inputs. A single-ended input uses two wires: input and ground. The measured input voltage is the difference between these two wires. A differential input uses three wires: input(+), input(–) and ground. The measured input voltage is the difference between the (+) and (–) inputs.

Differential inputs are frequently used either when the grounds of the input device and the measurement device (Athena III) are at different voltages, or when a low-level signal is being measured that has its own ground wire. A differential input also has higher noise immunity than a single-ended input because most noise affects both (+) and (–) input wires equally, so the noise is canceled out in the measurement. The disadvantage of differential

inputs is that only half as many are available because two input pins are required to produce a single differential input. Athena III can be configured for either 16 single-ended inputs, or eight differential inputs, as shown below.

A/D Single-ended/Differential Selection



The default setting is single-ended mode.

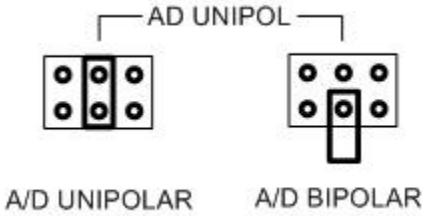
If you have a combination of single-ended and differential input signals, select differential mode. To measure the single-ended signals connect the signal to the plus (+) input and connect analog ground to the minus (–) input.

> ***WARNING:*** The maximum range of voltages that can be applied to an analog input on Athena III without damage is ±35V. If you connect the analog inputs on Athena to a circuit whose ground potential plus maximum signal voltage exceeds ±35V, the analog input circuit may be damaged. Check the ground difference between the input source and Athena III before connecting analog input signals.

7.5.2 Unipolar/Bipolar Input Settings

The analog inputs can be configured for either unipolar (positive input voltages only), or bipolar (both positive and negative input voltages). For unipolar inputs, install a jumper as shown below. For bipolar inputs, omit the jumper. The default configuration is bipolar mode (jumper out).

A/D Unipolar/Bipolar Selection



7.5.3 Analog Output Configuration Settings

The four analog outputs can also be configured for unipolar (positive voltages only) or bipolar (both positive and negative output voltages). In unipolar mode, the outputs range between 0-10V and the outputs reset to the bottom of their range (zero-scale). In bipolar mode, the outputs range between ±10V and the outputs reset to the middle of their range (mid-scale).

Normally, the D/A is configured to power up to 0V. When the power is turned on, the device connected to the analog output does not see a step change in voltage. Therefore, for unipolar mode, the outputs should normally be configured for zero-scale reset, and for bipolar mode the outputs should be configured for mid-scale reset because 0V is halfway between -10V and +10V, for the ±10V range.

The analog output configuration is set in software using the DACPOLEN and DACPOL registers. DACPOLEN must be set to 1. Then DACPOL can be used to set the analog outputs to unipolar (DACPOL = 0) or bipolar (DACPOL = 1) mode.

8. SYSTEM OPERATION

8.1 System Resources

The table below lists the system resources utilized by the circuits on Athena III.

Device	*Default Address*	*ISA IRQ*	*ISA DMA*	*Selectable Addresses*
Serial Port COM1	I/O 0x3F8 – 0x3FF	3.4	–	2F8, 3E8, 2E8
Serial Port COM2	I/O 0x2F8 – 0x2FF	3,4	–	3F8, 3E8, 2E8
Serial Port COM3	I/O 0x3E8 – 0x3EF	3,4,5,6,9	–	–
Serial Port COM4	I/O 0x2E8 – 0x2EF	3,15	–	–
LPT Printer Port	I/O 0x378 – 0x37F	5,7	3	278, 3BC
IDE Controller A	I/O 0x1F0 – 0x1F7	14	–	–
A/D Circuit (when applicable)	I/O 0x280 – 0x28F	4,5,6	–	–
Watchdog Timer/Serial Port/FPGA	I/O 0x25C-0x25F	–	–	–
Ethernet	OS-dependent	OS-dependent	–	–
USB	OS-dependent	OS-dependent	–	–
Sound	OS-dependent	OS-dependent	–	–
Video	OS-dependent	OS-dependent	–	–

Note: In the preceding table, the selectable addresses are declared in CMOS BIOS.

Most of these resources are configurable and, in many cases, the Operating System alters these settings. The main devices that are subject to this dynamic configuration are on-board Ethernet, sound, video, USB, and any PC/104-*Plus* cards that are in the system. These settings may also vary depending on what other devices are present in the system. For example, adding a PC/104-*Plus* card may change the on-board Ethernet resources.

The serial port settings for COM3 and COM4 are jumper-selectable (JP7), whereas the settings for COM1 and COM2 are entirely software-configured in the BIOS.

8.2 Console Redirection to a Serial Port

In many applications without a local display and keyboard, it may be necessary to obtain keyboard and monitor access to the CPU for configuration, file transfer, or other operations. Athena III supports this operation by enabling keyboard input and character output onto a serial port, referred to as console redirection. A serial port on another PC can be connected to the serial port on Athena III with a null modem cable, and a terminal emulation program, such as HyperTerminal, can be used to establish the connection. The terminal program must be capable of transmitting special characters including F2 (some programs or configurations trap special characters).

The default Athena III BIOS setting disables console redirection.

There are three possible configurations for console redirection:

- POST-only (default)
- Always On
- Disabled

To modify the console redirection settings:

1. Enter the BIOS.
2. Select the Advanced menu.
3. Select Serial Port Console Redirection.
4. In Com Port Address, select Disabled to disable the function, On-board COM A for COM1, or On-board COM B for COM2 (default).

If you select Disabled, you will not be able to enter BIOS again during power-up through the serial port.

To reenter BIOS when console redirection is disabled, you must install a video monitor or LCD and use a keyboard. Erasing the CMOS RAM returns the BIOS to its default settings.

Note: Before erasing CMOS RAM, write down any custom BIOS settings you have made.

If you selected COMA or COMB, continue with the configuration, as follows.

1. For Console Type, select PC ANSI.
2. You can modify the baud rate and flow control here if desired.
3. At the bottom, for Continue C.R. after POST, select Off (default) to turn off after POST or select On to remain on always.
4. Exit the BIOS and save your settings.

8.3 Flash Memory

Athena III contains a 2048KB, 16-bit wide flash memory chip for storage of BIOS and other system configuration data.

8.4 System Reset

Athena III contains a chip to control system reset operation. Reset occurs under the following conditions.

- User causes reset with a ground contact on the *Reset* input
- Input voltage drops below 4.75V
- Over-current condition on output power line

The ISA Reset signal is an active high pulse with a 200ms duration. The PCI Reset is active low, with a typical pulse width duration of 200 msec.

9. BIOS

Athena III uses a BIOS from American Megatrends modified to support the custom features of the Athena III SBC.

9.1 BIOS Settings

To change the following BIOS settings, press F2 during system startup power on self-test (POST).

9.1.1 Serial Ports

The address and interrupt settings for serial ports COM1 and COM2 may be modified. COM1 and COM2 address and interrupt settings are configured using the Advanced, Advanced Chipset Control, I/O Chip Device Configuration menu.

The addresses of COM3 and COM4 are fixed. The IRQ selections for COM3 and COM4 are configured using jumper block JP6.

9.1.2 Parallel Port

The parallel port is configured using the Advanced, I/O Chip Device Configuration menu. The port is set by default to ECP mode and located at address 0x378, IRQ 7 and DMA 3.

9.1.3 LCD Video Settings

Athena provides direct digital support for LVDS-based LCD interfaces only. As such, there are two settings that affect this support during BIOS boot.

Boot Video Device – By default, this is set to “AUTO”. With the AUTO setting, the system attempts to identify an RGB monitor (via DDC). If no RGB monitor is detected, the system enables LCD support. If you choose to use the LCD display regardless of standard monitor connection (i.e., with both connected at once), set “Boot Video Device” to “Both”.

Panel Type – This setting defaults to “7”. Do not alter this setting unless specifically instructed to do so. This setting affects the LCD display modes supported; mode “7” is the only setting currently supported. Not all LCD displays are supported.

9.1.4 Miscellaneous Settings

- Memory Cache

  Unless there is a specific reason to change these settings, it is best to keep these settings as-is. Certain system functions, such as USB keyboard support under BIOS menus, may be adversely affected by changes to these settings. These cache settings can make a noticeable difference for low-level BIOS calls and, as such, can severely limit performance if they are disabled.

- Advanced Chipset Control

  The following settings should be retained:

  Frame Buffer Size: 8MB

  AGP Rate: 4X

  Expansion Bus Performance: Normal

The Frame Buffer size can be increased for specific applications. Be aware, however, that an increase in this memory size will result in a decrease in overall system memory available. The AGP rate affects internal video accesses and does not affect any external bus speeds.

“Expansion Bus Performance” is an adjustment to allow an increase in ISA I/O Access speeds. For applications where ISA I/O accesses seem to be a limiting factor, this performance may be increased to “Accelerated”. Be aware that increasing these timings may adversely affect system stability with external add-on PC/104 cards. This setting has no direct affect on PCI or memory speeds; it only affects ISA PC/104 devices. It is best to leave this setting at “Normal,” if there are no ISA I/O performance issues.

- Advanced

  Installed O/S: Select the operating system.

  Large Disk Access Mode: Select the disk access mode.

- On-Chip Multifunction Device

  USB Device: Enabled/disable USB ports.

  Legacy Audio:

  "Legacy Audio" only affects DOS-based applications when used with the VIA-supported DOS Drivers. Enabling this setting will require system I/O, IRQ, and DMA resources. It is strongly recommended that this setting be left "Disabled."

- PCI and ISA Configuration (from the Advanced menu)

  The following settings should be retained:

  PCI IRQ Level 1-4: Auto-select for all

  PCI/PNP ISA UMB Region Exclusion: Available for all

- Power Management

  This setting is only effective under DOS. Otherwise, the OS power management settings pre-empt these settings. The only power management mode supported by the system is "Power-On Suspend." Other suspend modes are not supported and should not be used under any OS. Examples of unsupported suspend modes include, "Hibernate," under Windows, and "Suspend-to-Disk" or "Suspend-to-RAM".

- Memory Shadow

  These parameters should only be modified by advanced users. These settings can adversely affect system performance and reliability.

9.2 BIOS Console Redirection Settings

For applications where the Video interfaces are not used, the textual feedback typically sent to the monitor can be redirected to a COM port. In this manner, a system can be managed and booted without using a video connection.

The BIOS allows the following configuration options for Console Redirection to a COM port.

- COM port address: Disabled (default), COM port A, or COM port B.

  If Console Redirection is enabled here, the associated COM port (with "A" here referring to COM 1 and "B" referring to COM 2) is enabled regardless of the COM port settings elsewhere.
- "Continue CR after POST": Off (default), or On.
- Determines whether or not the system is to wait for a carriage return over the COM port before continuing (after POST is completed and before OS starts loading).
- Baud Rate: 19.2K (default), 300, 1200, 2400, 9600, 38.4K, 57.6K, 115.2K.
- Console Connection: Direct (default) or Modem.
- Console Type: PC ANSI (default), VT100, VT100 (8-bit), PC-ANSI (7-bit), VT100+, or VT-UTF8.
- Flow Control: CTS/RTS (default), XON-XOFF, None.
- Number of video Pages to support: 1(default) to 8.

Note: Console Redirection only works for text-based interaction. If the OS enables video and starts using direct video functions (which would be the case with a Linux X-terminal or Windows, for example), Console Redirection has no effect and video is then required.

10. SYSTEM I/O

10.1 Ethernet

Athena III provides a Gigabit Ethernet port derived from an Intel 82574ITMAC/PHY connected via PCIe from the Tunnel Creek I/O hub. A gigabit magnetic chip and header complete the circuit.

The Athena III Software CD includes Ethernet drivers for Windows XP, Windows CE, and Linux. The latest drivers can also be downloaded from National Semiconductor's website, listed in the Additional Information section of this document. (Search for "DP83815" to locate the product folder on the website).

A DOS utility program is provided for testing the chip and accessing the configuration EEPROM. Each board is factory-configured for a unique MAC address using this program. To run the program, boot the computer to DOS because the program will not run properly in a DOS window. In normal operation this program is not required.

Additional software support includes a packet driver with software to allow a full TCP/IP implementation.

10.2 Serial Ports

Athena III contains four serial ports. Each port is capable of transmitting at speeds up to 115.2Kbaud. Ports COM1 and COM2 are built into the standard chipset, which are standard 16550 UARTs with 16-byte FIFOs.

Ports COM3 and COM4 are derived from an Exar 16C2850 dual UART chip and include 128-byte FIFOs. These ports may be operated at speeds to 1.5Mbaud with installation of high-speed drivers, as a custom option.

The serial ports use the following default system resources.

Port	*I/O Address Range*	*IRQ*
COM1	0x3F8 - 0x3FF	4
COM2	0x2F8 - 0x2FF	3
COM3	0x3E8 - 0x3EF	3,4,5,6,9
COM4	0x2E8 - 0x2EF	3,15

The COM1 and COM2 settings may be changed in the system BIOS. Select the *Advanced* menu, followed by *I/O Device Configuration,* to modify the base address and interrupt level.

The addresses of COM3 and COM4 are fixed. The IRQ settings for COM3 and COM4 are selected using jumper block J10. COM3 can use IRQ3, IRQ4, IRQ5, IRQ6 or IRQ9, and COM4 can use IRQ3 or IRQ15, as described in the Board Configuration section of this document.

Note: Once these jumper selections are made, the user must update the Serial Port IRQ settings to match these selections. The IRQ settings are NOT auto detected in the same way as the address settings.

10.3 USB Ports

Four USB 2.0 ports, USB0 through USB3, are accessible using cable assemblies attached to connector J15 and J16.

USB support is intended primarily for the following devices (although any USB-standard device should function).

- Keyboard
- Mouse
- USB Floppy Drive (This is required for Crisis Recovery of boot ROM)
- USB flash disk

The BIOS supports the USB keyboard during BIOS initialization screens and legacy emulation for DOS-based applications.

The USB ports can be used for keyboard and mouse at the same time that the PS/2 keyboard and mouse are connected.

11. NOTES ON OPERATING SYSTEMS AND BOOTING PROCEDURES

11.1 Windows Operating System Installation

Windows operating systems installation should follow these steps, or some device drivers may not function correctly under Windows.

1. Enable CD-ROM support in the BIOS. Change the boot sequence in the BIOS so the system boots from CD-ROM first.
2. Insert the Windows installation CD into the CD-ROM and restart the computer.
3. Follow the manufacturer's instructions for installing Windows.

11.1.1 Driver Installation

Drivers are provided on a CD. Please, follow the instructions included on the CD to install drivers for the different operating systems.

11.1.2 BIOS Setting for Windows

When using any version of Windows, the Operating System selection in the BIOS setup menus should be set to Win98. Also, *Legacy Audio* must be disabled for Windows to boot properly.

11.2 DOS Operating Systems Installation

User the following sequence to install DOS operating systems: MS-DOS, FreeDOS and ROM-DOS.

1. Enable the following in BIOS:
    - Floppy Drive detection
    - Legacy USB support
2. Change the BIOS boot sequence so the system boots through the USB floppy drive.
3. Insert the DOS installation floppy disk into the USB floppy drive and start/restart the system.
4. Install any drivers needed.

    Note: For DOS Ethernet, set **Operating System** to **other** in the BIOS.

    Note: DOS Sound emulation is currently not functional.

12. DATA ACQUISITION CIRCUIT

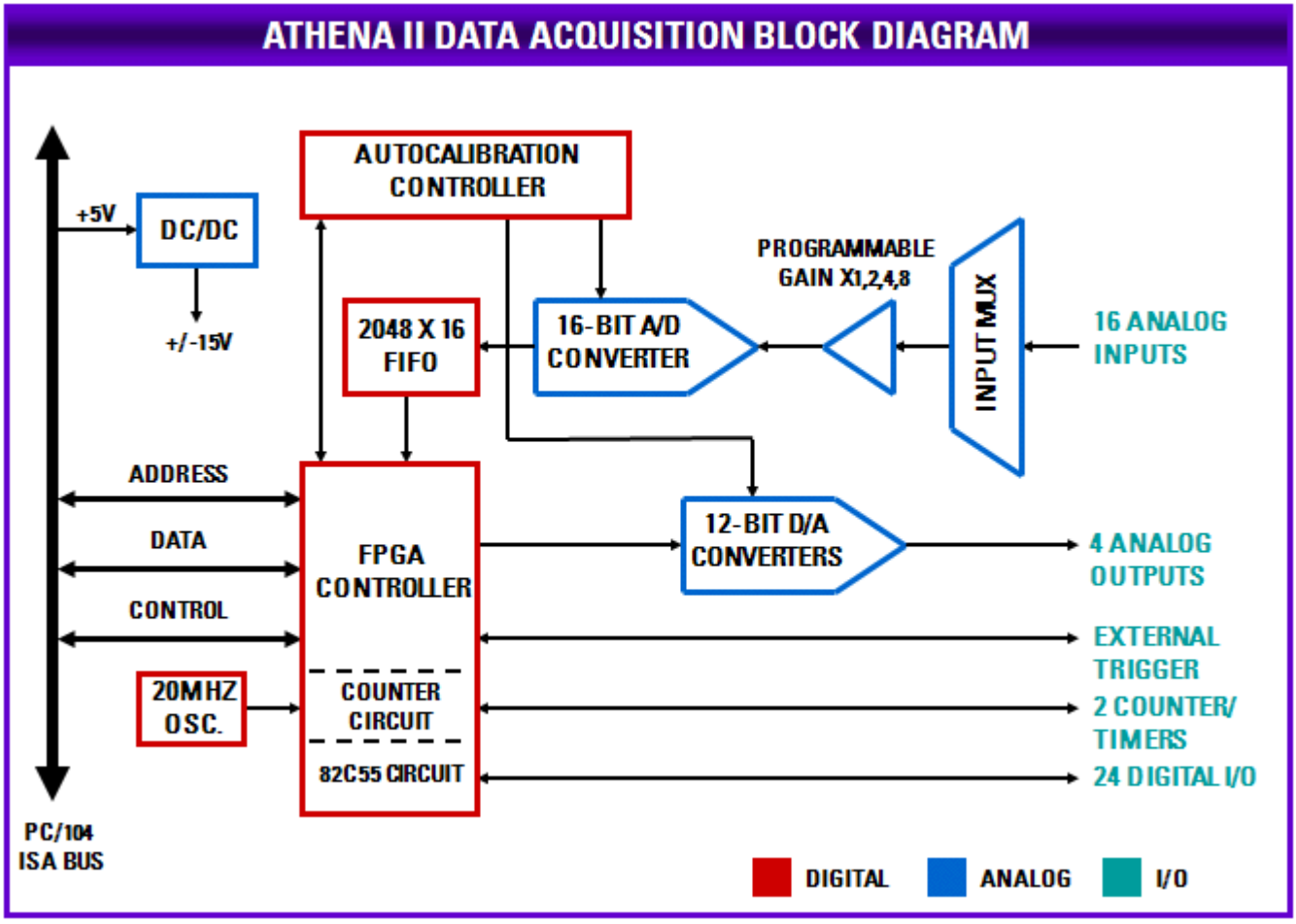
Athena III contains a data acquisition subsystem consisting of A/D, D/A, digital I/O, and counter/timer features. This subsystem is equivalent to a complete add-on data acquisition module.

The A/D section includes a 16-bit A/D converter, 16 input channels, and a 2048-sample FIFO. Input ranges are programmable, and the maximum sampling rate is 200KHz. The D/A section includes four 12-bit D/A channels. The digital I/O section includes 24 lines with programmable direction. The counter/timer section includes a 24-bit counter/timer to control A/D sampling rates and a 16-bit counter/timer for user applications.

High-speed A/D sampling is supported with interrupts and a FIFO. The FIFO is used to store a user-selected number of samples, and the interrupt occurs when the FIFO reaches this threshold. Once the interrupt occurs, an interrupt routine runs and reads the data out of the FIFO. In this way the interrupt rate is reduced by a factor equal to the size of the FIFO threshold, enabling a faster A/D sampling rate. The circuit can operate at sampling rates of up to 200KHz, with an interrupt rate of 6.6-10KHz.

The A/D circuit uses the default (hard wired) setting of I/O base address 280h and IRQ 5. The IRQ setting can be changed if needed. The interrupt level is changed with jumper block JP7 and also with the IRQ number in the BIOS.

The figure on the next page shows a block diagram of the data acquisition circuit.



12.1 Data Acquisition Circuitry I/O Map

12.1.1 Overview

The data acquisition circuitry on Athena III occupies 16 bytes in I/O memory space. The default address range is 280h (base address) to 28Fh.

The data acquisition FPGA can be enabled/disabled in the BIOS under the Advanced menu. Scroll down to the "FPGA Mode" option and select "Enabled" or "Disabled," accordingly. If the FPGA is disabled you will not be able to interact with the data acquisition circuit. The FPGA can also be enabled or disabled programmatically through the CPLD.

12.1.2 Register Map Page Summary

The following table summarizes the DAC register functions. The registers are paged to allow access to enhanced functions. There are three register pages and the desired page is selected using the A/D gain and scan settings register, Base+3, bits PG0-PG1, provided the board is in enhanced mode.

Page 0		
Base +	**Write Function**	**Read Function**
0	Command	A/D LSB
1	Enhanced mode control	A/D MSB
2	A/D channel	A/D channel
3	A/D gain/page select/scan settings	A/D gain and status
4	Interrupt/DMA/counter control	Interrupt/DMA/counter control
5	FIFO threshold	FIFO threshold
6	DAC LSB	FIFO depth
7	DAC MSB + channel no.	Analog operation status
8	Digital I/O port A	Digital I/O port A
9	Digital I/O port B	Digital I/O port B
10	Digital I/O port C	Digital I/O port C
11	Digital I/O control	Digital I/O control
12	Counter/timer D7-0	Counter/timer D7-0
13	Counter/timer D15-8	Counter/timer D15-8
14	Counter/timer D23-16	Counter/timer D23-16
15	Counter/timer control	FPGA revision code

Page 1		
Base +	**Write Function**	**Read Function**
12	Trim DAC data/EEM data	EEM data
13	EEPROM command/Trim DAC	EEM command address
14	Auto-CAL/Trim DAC	Trim DAC/EEM/Auto-Cal status
15	Write enable	Page 1 select read back check

Page 2		
Base +	**Write Function**	**Read Function**
12	ADC expanded FIFO	ADC expanded FIFO
13	ADC control	ADC control
14	-	-
15	-	Page 2 select read back check

Note 1: Page 0, registers 0-11 are accessible when Page 1 or Page 2 are selected.

Note 2: In the following tables, blank bits are not used. Writes to a blank bit have no effect and reads from a blank bit return a value of zero.

12.1.3 Register Map Bit Summary

Page 0 Write Register Summary

Base +	7	6	5	4	3	2	1	0
0	STARTAD	RSTBRD	RSTDA	RSTFIFO	CLRDMA	CLRT	CLRD	CLRA
1							PG1	PG0
2	H3	H2	H1	H0	L3	L2	L1	L0
3	-	-	PG1	PG0	-	SCANEN	ADG1	ADG0
4	CKSEL1	FRQSEL1	FRQSEL0	ADCLK	-	TINTE	DINTE	AINTE
5	- / FT10	- / FT09	FT5/ FT08	FT4/ FT07	FT3/ FT06	FT2/ FT05	FT1/ FT04	FT0/ FT03
6	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
7	DACH1	DACH0	-	-	DA11	DA10	DA9	DA8
8	A7	A6	A5	A4	A3	A2	A1	A0
9	B7	B6	B5	B4	B3	B2	B1	B0
10	C7	C6	C5	C4	C3	C2	C1	C0
11	DIOCTR		DASIM	DIRA	DIRCH	-	DIRB	DIRCL

Page 0 Read Register Summary

Base +	7	6	5	4	3	2	1	0
0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
2	H3	H2	H1	H0	L3	L2	L1	L0
3	ADBUSY	SE/DIFF	ADWAIT	DACBSY	OVF	SCANEN	ADG1	ADG0
4	CKSEL1	FRQSEL1	FRQSEL0	ADCLK	DMAEN	TINTE	DINTE	AINTE
5	- / FD07	-/ FD06	FT5/FD05	FT4/FD04	FT3/FD03	FT2/FD02	FT1/FD01	FT0/FD00
6	FD7/FD11	FD6/FD10	FD5/FD09	FD4/FD08	FD3/OVF	FD2/FF	FD1/HF	FD0/EF
7	DMAINT	TINT	DINT	AINT	ADCH3	ADCH2	ADCH1	ADCH0
8	A7	A6	A5	A4	A3	A2	A1	A0
9	B7	B6	B5	B4	B3	B2	B1	B0
10	C7	C6	C5	C4	C3	C2	C1	C0
11	DIOCTR		DASIM	DIRA	DIRCH	-	DIRB	DIRCL

Page 1 Write Register Summary

Base +	7	6	5	4	3	2	1	0
12	CtrD7	CtrD6	CtrD5	CtrD4	CtrD3	CtrD2	CtrD1	CtrD0
13	CtrD15	CtrD14	CtrD13	CtrD12	CtrD11	CtrD10	CtrD9	CtrD8
14	CtrD23	CtrD22	CtrD21	CtrD20	CtrD19	CtrD18	CtrD17	CtrD16
15	CTRNO	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR

Page 1 Read Register Summary

Base +	7	6	5	4	3	2	1	0
12	D7	D6	D5	D4	D3	D2	D1	D0
13	A7	A6	A5	A4	A3	A2	A1	A0
14	-	TDBUSY	EEBUSY	CALMUX	-	-	-	-
15	-- 0xA1 --							

Page 2 Write Register Summary

Base +	7	6	5	4	3	2	1	0
12	-	-	-	-	-	-	-	EXFIFO
13	-	-	DACPOLE	DACPOL	ADPOL	ADPOLEN	ADSD	ADSDEN
14	-	-	-	-	-	-	-	SCANINT
15	DAQ_LED	-	-	-	-	-	-	-

Page 2 Read Register Summary

Base +	7	6	5	4	3	2	1	0
12	-	-	-	-	-	-	-	EXFIFO
13	-	-	DACPOLEN	DACPOL	ADPOL	ADPOLEN	ADSD	ADSDEN
14								SCANINT
15	-- 0xA2 --							

12.2 Main Registers

Base + 0 Write Command Register

Bit No.	7	6	5	4	3	2	1	0
Name	STRTAD	RSTBRD	RSTDA	RSTFIFO	CLRDMA	CLRT	CLRD	CLRA
Reset	X	X	X	X	X	X	X	X

This register is used to perform various functions. The register bits are not data bits but instead command triggers. Each function is initiated by writing a 1 to a particular bit. **Writing a 1 to any bit in this register does not affect any other bit in this register.** For example, to reset the FIFO, write the value 0x10 (16) to this register to write a 1 to bit 4. No other function of the register will be performed. Multiple actions can be carried out simultaneously by writing a 1 to multiple bits simultaneously.

STRTAD Start an A/D conversion (trigger the A/D) when in software-trigger mode (AINTE = 0). Once the program writes to this bit, the A/D conversion will start and the STS bit (base + 3 bit 7) will go high. The program should then monitor STS and wait for it to go low (check if value in base + 3 is less than 128 or 0x80). When it goes low the A/D data at Base + 0 and Base + 1 may be read.

When AINTE = 1 (base + 4 bit 0), the A/D cannot be triggered by writing to this bit. Instead the A/D will be triggered by a signal selected by ADCLK in base + 4 bit 5.

RSTBRD Reset the entire board excluding the D/A. Writing a 1 to this bit causes all registers on the board to be reset to 0. The effect on the digital I/O is that all ports are reset to input mode, and the logic state of their pins will be determined by the pull-up/pull-down configuration setting selected by the user. All A/D, counter/timer and interrupt functions will cease. However the D/A values will remain constant.

RSTDA Reset the 4 analog outputs. The analog outputs will be reset to zero volts.

RSTFIFO Reset the FIFO depth to 0. This clears the FIFO so that further A/D conversions will be stored in the FIFO starting at address 0.

CLRDMA Writing a 1 to this bit causes the DMA interrupt request flip flop to be reset.

CLRT Writing a 1 to this bit causes the timer interrupt request flip flop to be reset.

CLRD Writing a 1 to this bit causes the digital I/O interrupt request flip flop to be reset.

CLRA Writing a 1 to this bit causes the analog interrupt request flip flop to be reset.

The user's interrupt routine must write to the appropriate bit prior to exiting in order to enable future interrupts. Otherwise the interrupt line will stay high indefinitely and no additional interrupt requests will be generated by the board.

Base + 0 Read A/D LSB

Bit No.	7	6	5	4	3	2	1	0
Name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Reset	0	0	0	0	0	0	0	0

AD7 - 0 A/D data bits 7 - 0; AD0 is the LSB; A/D data is an unsigned 16-bit value.

The A/D value is derived by reading two bytes from Base + 0 and Base + 1 and applying the following formula:

A/D value = (Base + 0 value) + (Base + 1 value) * 256

The value is interpreted as a twos complement 16-bit number ranging from –32768 to +32767. This raw A/D value must then be converted to the corresponding input voltage and/or the engineering units represented by that voltage by applying additional application-specific formulas. Both conversions (conversion to volts and then conversion to engineering units) may be combined into a single formula for efficiency.

Base + 1 Write Enhanced Features Access Register

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	PG1	PG0
Reset	0	0	0	0	0	0	0	0

This register has dual function. When 0xA5 and 0xA6 is written to this register nothing happens and the page bits PG1-0 are preserved. The 0xA5, 0xA6 functionality is kept to provide backward compatibility with existing code. In order to change the page, the PG1-0 bits should be changed. These bits are duplication of the page bits in Base + 3 register.

This register is different than in Athena-II and provides faster performance to access registers in other pages.

Page Select (0 - 2): Accessible any time to select any of the 3 pages.

Base + 1 Read A/D MSB

Bit No.	7	6	5	4	3	2	1	0
Name	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Reset	0	0	0	0	0	0	0	0

AD15 - 8 A/D data bits 15 – 8; AD15 is the MSB; A/D data is an unsigned 16-bit value.

See Base + 0 Read on the previous page for information on A/D values and formulas.

Base + 2 Read/Write A/D Channel Register

Bit No.	7	6	5	4	3	2	1	0
Name	H3	H2	H1	H0	L3	L2	L1	L0
Reset	0	0	0	0	0	0	0	0

H3 – H0 High channel of channel scan range

Ranges from 0 to 15 in single-ended mode, 0 - 7 in differential mode.

L3 - L0 Low channel of channel scan range

Ranges from 0 to 15 in single-ended mode, 0 - 7 in differential mode.

The high channel must be greater than or equal to the low channel.

When this register is written, the current A/D channel is set to the low channel so that the next time an A/D conversion is triggered the low channel will be sampled.

When this register is written to, the WAIT bit (Read Base + 3 bit 5) will go high for 10 microseconds to indicate that the analog input circuit is settling. During this time an A/D conversion should not be performed because the data will be inaccurate. After writing a new gain setting (Base + 3), the ADWAIT bit is also set, and the program must monitor it prior to starting an A/D conversion. The channel and gain registers can be written to in succession without waiting for the intervening ADWAIT signal. Only one ADWAIT period must be observed between the last triggering condition (write to Base + 2 or Base + 3) and the start of an A/D conversion.

The A/D circuit is designed to automatically increment the A/D channel each time a conversion is generated. This enables the user to avoid having to write the A/D channel each time. The A/D channel will rotate through the values between LOW and HIGH. For example, if LOW = 0 and HIGH = 3, the A/D channels will progress through the following sequence: 0, 1, 2, 3, 0, 1, 2, 3, 0, 1, ….

Reading from this register returns the value previously written to it.

Base + 3 **Write** **Analog Input Gain / Page Control**

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	PG1	PG0	X	SCANEN	ADG1	ADG0
Reset	0	0	0	0	0	0	0	0

PG1-PG0 Page Select (0 - 2): Only accessible when the board is configured on Enhanced Mode. When the board is on standard mode, only page 0 can be accessed.

SCANEN Scan mode enable:

1 Each A/D trigger will cause the board to generate an A/D conversion on each channel in the range LOW – HIGH (the range is set with the channel register in Base + 2). The STS bit (read Base + 3 bit 7) stays high during the entire scan. The time between A/D samples is determined by the SCANINT bit in page 2. If SCANINT=0, the scan interval is 10us, and if SCANINT=1, the scan interval is 5us.

0 Each A/D trigger will cause the board to generate a single A/D conversion on the current channel. The internal channel pointer will increment to the next channel in the range LOW – HIGH or reset to LOW if the current channel is HIGH. The STS bit stays high during the A/D conversion.

ADG1-0 Analog input gain. The gain is the ratio of the voltage seen by the A/D converter and the voltage applied to the input pin. The gain setting is the same for all input channels.

When this register is written to, the ADWAIT bit (Read Base + 3 bit 5) will go high for 10 microseconds to indicate that the analog input circuit is settling. During this time an A/D conversion should not be performed because the data will be inaccurate. After writing a new gain setting, the program should monitor the ADWAIT bit prior to starting an A/D conversion.

After writing a new channel selection (Base + 2), the ADWAIT bit is also set, and the program must monitor it prior to starting an A/D conversion.

The channel and gain registers can be written to in succession without waiting for the intervening ADWAIT signal. Only one ADWAIT period must be observed between the last triggering condition (write to Base + 2 or Base + 3) and the start of an A/D conversion.

The following table lists the possible analog input ranges:

ADG1	ADG0	Gain	Unipolar Range	Bipolar Range
0	0	1	0-10V	±10V
0	1	2	0-5V	±5V
1	0	4	0-2.5V	±2.5V
1	1	8	0-1.25V	±1.25V

Base + 3 **Read** **Analog Input Status**

Bit No.	7	6	5	4	3	2	1	0
Name	ADBUSY	SE/DIFF	ADWAIT	DACBSY	OVF	SCANEN	ADG1	ADG0
Reset	0	1	0	0	0	0	0	0

ADBUSY A/D Busy. 1 = A/D conversion or scan in progress, 0 = A/D is idle.

If SCANEN = 0 (single conversion mode), ADBUSY goes high when an A/D conversion is started and stays high until the conversion is finished. If SCANEN = 1 (scan mode enabled), ADBUSY stays high during the entire scan. After starting a conversion in software, the program must monitor ADBUSY and wait for it to become 0 prior to reading A/D values from Base + 0 and Base + 1.

SE/DIFF Single-ended / Differential mode indicator. 1 = Single Ended, 0 = Differential.

ADWAIT A/D input circuit status. 1 = A/D circuit is settling on a new value, 0 = ok to start conversion.

ADWAIT goes high after the channel register (Base + 2) or the gain register (Base + 3) is changed. It stays high for 9 microseconds. The program should monitor this bit after writing to either register and wait for it to become 0 prior to starting an A/D conversion.

DACBSY Indicates the DAC is busy updating (approx. 30 µS). 1 = Busy, 0 = Idle. Do not attempt to write to the DAC (registers 6 and 7) while DACBSY = 1.

OVF FIFO Overflow bit. This bit indicates that the FIFO has overflowed, meaning that the A/D circuit has attempted to write data to it when it is full. This condition occurs when data is written into the FIFO faster than it is read out.

When overflow occurs, the FIFO will not accept any more data until it is reset. The OVF condition is sticky, meaning that it remains true until the FIFO is reset, so the application program will be able to determine if overflow occurs. If overflow occurs, then you must either reduce the sample rate or increase the efficiency of your interrupt routine and/or operating system.

SCANEN Scan mode readback (see Base + 3 Write above).

ADG1-0 A/D gain setting readback (see Base + 3 Write above).

Base + 4 Read/Write Interrupt / Counter Control

Bit No.	7	6	5	4	3	2	1	0
Name	CKSEL1	FRQSEL1	FRQSEL0	ADCLK	DMAEN	TINTE	DINTE	AINTE
Reset	0	0	0	0	0	0	0	0

CKSEL1 Clock source selection for counter/timer 1:

0 = internal oscillator, frequency selected by CLKFRQ1

1 = external clock input CLK1 (DIO C pins must be set for ctr/timer signals)

FRQSEL1 Input frequency selection for counter/timer 1 when CKSEL1 = 1:

0 = 10MHz, 1 = 100KHz

FRQSEL0 Input frequency selection for counter/timer 0.

0 = 10MHz, 1 = 1MHz

ADCLK A/D trigger select when AINTE = 1:

0 = internal clock output from counter/timer 0

1 = external clock input EXTTRIG

DMAEN Enable DMA operation. 1 = enable, 0 = disable.

TINTE Enable timer interrupts. 1 = enable, 0 = disable.

DINTE Enable digital I/O interrupts. 1 = enable, 0 = disable.

AINTE Enable analog input interrupts. 1 = enable, 0 = disable.

NOTE: When AINTE = 1, the A/D cannot be triggered by writing to Base + 0.

Analog output interrupts are not supported on this board.

Multiple interrupt operations may be performed simultaneously. All interrupts will be on the same interrupt level. The user's interrupt routine must monitor the status bits to know which circuit has requested service. After processing the data but before exiting, the interrupt routine must then clear the appropriate interrupt request bit using the register at Base + 0.

Base + 5 **Write** **FIFO Threshold / FIFO Threshold X8**

Bit No.	7	6	5	4	3	2	1	0
Name	X/FT10	X/FT09	FT5/FT08	FT4/FT07	FT3/FT06	FT2/FT05	FT1/FT04	FT0/FT03
Reset	0	0	0	0	0	0	0	0

FT5–0 When EXFIFO = 0 (Basic Mode, See Register Description for Page 2 Base+12)

FIFO threshold. When the number of A/D samples in the FIFO reaches this number, the board will generate an interrupt and set AINT high (Base + 7 bit 4).

The valid range is 1-48. If the value written is greater than 48, then 48 will be used. If the value written is 0, then 1 will be used.

FT10–03 When EXFIFO = 1 (Enhanced Mode, See Register Description for Page 2 Base+12)

FIFO threshold (upper 8 of 11 bits). When the number of A/D samples in the FIFO reaches this number, the board will generate an interrupt and set AINT high (Base + 7 bit 4).

The valid range is 8 – 2048 in steps of 8. When EXFIFO is set to 1 for the first time the FIFO threshold is set automatically to 1024.

The interrupt routine is responsible for reading the correct number of samples out of the FIFO. The interrupt rate is equal to the total sample rate divided by the FIFO threshold. Generally, for higher sampling rates a higher threshold should be used to reduce the interrupt rate. However remember that the higher the FIFO threshold, the smaller the amount of FIFO space remaining to store data while waiting for the interrupt routine to respond. If you get a FIFO overflow condition, you must lower the FIFO threshold and/or lower the A/D sampling rate.

Base + 5 **Read** **FIFO Threshold / FIFO Depth LSB**

Bit No.	7	6	5	4	3	2	1	0
Name	X/FD07	X/FD06	FT5/FD05	FT4/FD04	FT3/FD03	FT2/FD02	FT1/FD01	FT0/FD00
Reset	0	0	0	0	0	0	0	0

FT5-0 When EXFIFO = 0 (Basic Mode, See Register Description for Page 2 Base+12)
FIFO threshold. When the number of A/D samples in the FIFO reaches this number, the board will generate an interrupt and set AINT high (Base + 7 bit 4).

FD07-00 When EXFIFO = 1 (Enhanced Mode, See Register Description for Page 2 Base+12)

Current FIFO Depth LSB. This value indicates the lower 8 bits of the number of A/D values currently stored in the FIFO.

Base + 6 **Write** **DAC LSB**

Bit No.	7	6	5	4	3	2	1	0
Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
Reset	0	0	0	0	0	0	0	0

DA7–0 D/A data bits 7 - 0; This register stores the DA LSB. D/A data is an unsigned 12-bit value. This register must be written to before the MSB, since writing the MSB updates the DAC immediately. (Unless DASIM is enabled)

Base + 6 **Read** **A/D Channel and FIFO Status**

Bit No.	7	6	5	4	3	2	1	0
Name	FD7/FD11	FD6/FD10	FD5/FD09	FD4/FD08	FD3/OVF	FD2/FF	FD1/HF	FD0/EF
Reset	0	0	0	0	0	0	0	0

FD7–0 When EXFIFO = 0 (Basic Mode, See Register Description for Page 2 Base+12)

Current FIFO depth. This value indicates the number of A/D values currently stored in the FIFO.

FD11–08 When EXFIFO = 1 (Enhanced Mode, See Register Description for Page 2 Base+12)
Current FIFO depth MSB. This value indicates the upper 4 bits of the number of A/D values currently stored in the FIFO.

OVF FIFO Overflow bit. This bit indicates that the FIFO has overflowed, meaning that the A/D circuit has attempted to write data to it when it is full. This condition occurs when data is written into the FIFO faster than it is read out.

When overflow occurs, the FIFO will not accept any more data until it is reset. The OVF condition is sticky, meaning that it remains true until the FIFO is reset, so the application program will be able to determine if overflow occurs. If overflow occurs, then you must either reduce the sample rate or increase the efficiency of your interrupt routine and/or operating system.

FF FIFO Full Bit. The next conversion will result in an overflow.

HF FIFO Half Full Bit. FIFO is at least half full containing at least 1k words of A/D data.

EF FIFO Empty. FIFO is empty.

Base + 7 Write DAC MSB

Bit No.	7	6	5	4	3	2	1	0
Name	DACH1	DACH0	-	-	DA11	DA10	DA9	DA8
Reset	0	0	0	0	0	0	0	0

DACH1–0 D/A channel. The values written to Base + 6 and Base + 7 update the selected channel immediately unless DASIM is enabled. The update takes approximately 50ns due to the DAC serial interface.

DA11–8 D/A bits 11 - 8; DA11 is the MSB. D/A data is an unsigned 12-bit value. Writing to this register updates the DAC (If DASIM is disabled).

Base + 7 Read Analog Operation Status

Bit No.	7	6	5	4	3	2	1	0
Name	-	TINT	DINT	AINT	ADCH3	ADCH2	ADCH1	ADCH0
Reset	0	0	0	0	0	0	0	0

TINT Timer interrupt status, 1 = interrupt pending, 0 = interrupt not pending.

DINT Digital I/O interrupt status, 1 = interrupt pending, 0 = interrupt not pending.

AINT Analog input interrupt status, 1 = interrupt pending, 0 = interrupt not pending.

ADCH3-0 Current A/D channel. This is the channel that will be sampled on the **next** conversion.

When any of the bits 6–4 are 1, the corresponding circuit is requesting interrupt service. The interrupt routine must poll these bits to determine which circuit needs service and then act accordingly.

Base + 8 Read / Write Digital I/O Port A

Bit No.	7	6	5	4	3	2	1	0
Name	A7	A6	A5	A4	A3	A2	A1	A0
Reset	0	0	0	0	0	0	0	0

These registers are used for digital I/O on PortA. The direction of each register is controlled by the DIO control register at Base+11.

Base + 9 Read / Write Digital I/O Port B

Bit No.	7	6	5	4	3	2	1	0
Name	B7	B6	B5	B4	B3	B2	B1	B0
Reset	0	0	0	0	0	0	0	0

These registers are used for digital I/O on PortB. The direction of each register is controlled by the DIO control register at Base+11.

Base + 10 Read / Write Digital I/O Port C

Bit No.	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Reset	0	0	0	0	0	0	0	0

These registers are used for digital I/O on PortC. The direction of each register is controlled by the DIO control register at Base+11.

Base + 11 Write Digital I/O and DA Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	DIOCTR		DASIM	DIRA	DIRCH	-	DIRB	DIRCL
Reset	1	X	0	1	1	0	1	1

DIOCTR Selects counter I/O signals or digital I/O lines PL3B(7), PL3A(6), PL2B(5), PL2A(4) on the FPGA pins (Pins 21-24 on J23):

Pin No.	DIOCTR = 0	DIOCTR = 1
PL3B(7)	PC4Gate 0	DIO
PL3A(6)	PC5Gate 1	DIO
PL2B(5)	PC6 Clk 1	DIO
PL2A(4)	PC7 Out 0	DIO

NOTE: If DIOCTR = 1, then the pin direction is controlled by DIRCH.

This bit resets to 1.

DIRA Port A direction. 0 = output, 1 = input

DIRB Port B direction: 0 = output, 1 = input

DIRCH Port C bits 7-4 direction: 0 = output, 1 = input

DIRCL Port C bits 3-0 direction: 0 = output, 1 = input

DASIM DASIM D/A simultaneous update control. This bit determines when the D/A is updated.
0 = When Base+7 is written, the D/A data is loaded into the D/A and the update command is sent immediately afterwards.

1 = When Base+7 is written, the 12bit DA values will be loaded into the D/A converter but the update command will not be issued. Instead, a read of the register at Page 2, Base+15 will cause the update of the D/A converter.

Base + 11 Read Digital I/O and DA Control Register Readback

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	DASIM	DIRA	DIRCH	-	DIRB	DIRCL
Reset	0	0	0	0	0	0	0	0

Read-back of Base+11.

12.2.1 Page 0: Counter / Timer Control

Page 0, Base + 12 Read/Write Counter/Timer D7 - 0

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD7	CTRD6	CTRD5	CTRD4	CTRD3	CTRD2	CTRD1	CTRD0
Reset	0	0	0	0	0	0	0	0

This register is used for both Counter 0 and Counter 1. It is the LSB for both counters.

When writing to this register, an internal load register is loaded. Upon issuing a Load command through Base + 15, the selected counter's LSB register will be loaded with this value. When reading from this register, the LSB value of the most recent Latch command will be returned. The value returned is NOT the value written to this register.

Page 0, Base + 13 Read/Write Counter/Timer D15 - 8

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD15	CTRD14	CTRD13	CTRD12	CTRD11	CTRD10	CTRD9	CTRD8
Reset	0	0	0	0	0	0	0	0

This register is used for both Counter 0 and Counter 1. It is the MSB for counter 1 and the middle byte for counter 0.

When writing to this register, an internal load register is loaded. Upon issuing a Load command through Base + 15, the selected counter's associated register will be loaded with this value. For counter 0, it is the middle byte. For counter 1, it is the MSB.

When reading from this register, the associated byte of the most recent Latch command will be returned. The value returned is NOT the value written to this register.

Page 0, Base + 14 Read/Write Counter/Timer D23 - 16

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD23	CTRD22	CTRD21	CTRD20	CTRD19	CTRD18	CTRD17	CTRD16
Reset	0	0	0	0	0	0	0	0

This register is used for Counter 0 only. Counter 0 is 24 bits wide, while Counter 1 is only 16 bits wide.

When writing to this register, an internal load register is loaded. Upon issuing a Load command through Base + 15 for Counter 0, the counter's MSB register will be loaded with this value. When issuing a Load command for counter 1, this register is ignored.

When reading from this register, the MSB value of the most recent Latch command for counter 0 will be returned. The value returned is NOT the value written to this register.

Page 0, Base + 15 Write Counter/Timer Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	CTRNO	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR
Reset	0	0	0	0	0	0	0	0

This register is used to control the counter/timers. A counter is selected with bit 7, and then a 1 is written to any ONE of bits 6 – 0 to select the desired operation for that counter. The other bits and associated functions are not affected. Thus only one operation can be performed at a time.

CTRNO Counter no., 0 or 1

LATCH Latch the selected counter so that its value may be read. The counter must be latched before it is read. Reading from registers 12-14 returns the most recently latched value. If you are reading Counter 1 data, read only Base + 12 and Base + 13. Any data in Base + 14 will be from the previous Counter 0 access.

GTDIS Disable external gating for the selected counter.

GTEN Enable external gating for the selected counter. If enabled, the associated gate signal GATE0 or GATE1 controls counting on the counter. If the GATEn signal is high, counting is enabled. If the GATEn signal is low, counting is disabled.

CTDIS Disable counting on the selected counter. The counter will ignore input pulses.

CTEN Enable counting on the selected counter. The counter will decrement on each input pulse.

LOAD Load the selected counter with the data written to Base + 12 through Base + 14 or Base + 12 and Base + 13 (depending on which counter is being loaded).

CLR Clear the current counter (set its value to 0).

Page 0, Base + 15 Read FPGA Revision Code

Bit No.	7	6	5	4	3	2	1	0
Name	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0
Reset	0	0	0	0	0	0	0	0

REV7-0 Revision code, read as a 2-digit hex value. The first rev of this FPGA should be 0x48.

12.3 Page 1 Register Definitions

Page 1, Base + 12 Read/Write EEPROM / TrimDAC Data Register

Bit No.	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

During EEPROM or TrimDAC write operations, the data written to this register will be written to the selected device.

During EEPROM read operations this register contains the data to be read from the EEPROM and is valid after EEBUSY = 0.

The TrimDAC data cannot be read back.

D7-0 Calibration data to be read or written to the EEPROM and/or TrimDAC.

Page 1, Base + 13 Read/Write EEPROM / TrimDAC Address Register

Bit No.	7	6	5	4	3	2	1	0
Name	A7	A6	A5	A4	A3	A2	A1	A0

A7-A0 EEPROM / TrimDAC address.

The EEPROM recognizes address 0 – 255 using address bits A7 – A0. The TrimDAC only recognizes addresses 0 – 7 using bits A2 – A0. In each case remaining address bits will be ignored.

Page 1, Base + 14 Write Calibration Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	EE_EN	EE_RW	RUNCAL	CALMUX	TDACWR	X	X	X

This register is used to initiate various commands related to autocalibration.

EE_EN EEPROM Enable. Writing a 1 to this bit will initiate a transfer to/from the EEPROM as indicated by the EE_RW bit. If both EE_EN and TDACWR are set to '1' then TDACWR is ignored.

EE_RW Selects read or write operation for the EEPROM:

0 = Write

1 = Read

RUNCAL Writing 1 to this bit causes the board to reload the calibration settings from EEPROM. If this bit is set to 1, all other bits written to this register are ignored, however the current value of CALMUX is preserved.

CALMUX Calibration multiplexor enable. The cal mux is used to read precision on-board reference voltages that are used in the autocalibration process. It also can be used to read back the value of analog output 0.

1 = enable cal mux and disable user analog input channels

0 = disable cal mux, enable user inputs

TDACWR TrimDAC Write. Writing 1 to this bit will initiate a transfer to the TrimDAC addressed by the register at page 1, base+13. (used in the autocalibration process). If both EE_EN and TDACWR are set to '1' then TDACWR is ignored.

Page 1, Base + 14 Read Calibration Status Register

Bit No.	7	6	5	4	3	2	1	0
Name	0	TDBUSY	EEBUSY	CALMUX	0	0	0	0

TDBUSY TrimDAC busy indicator.

0 User may access TrimDAC

1 TrimDAC is being accessed; user must wait.

EEBUSY EEPROM busy indicator.

0 User may access EEPROM

1 EEPROM is being accessed; user must wait.

CALMUX Readback of calibration multiplexor enable setting:

1 Enabled.

0 Disabled.

Page 1, Base + 15 Write EEPROM Access Key Register

The user must write the key value 0xA5 (binary 10100101) to this register each time after any change in the states of registers bits PG1 and PG0 (base+1 bits 1-0) in order to get access to the EEPROM. This helps prevent accidental corruption of the EEPROM contents. Once the key value is written, access to the EEPROM remains enabled until the page bits are changed.

12.4 Page 2 Register Definitions

ADC Expanded FIFO: Base+12 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	-	-	-	ADCEXF

ADCEXF ADC expanded FIFO mode flag.

0 = Not in expanded FIFO mode.

1 = In expanded FIFO mode.

Note: When in expanded FIFO mode, the FIFO threshold and FIFO depth bits represent the upper eight bits of an 11-bit value.

ADC Expanded FIFO: Base+12 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	-	-	-	ADCEXF

ADCEXF ADC expanded FIFO mode flag.

0 = Not in expanded FIFO mode.

1 = In expanded FIFO mode.

ADC Control: Base+13 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	0	0	DACPOLEN	DACPOL	ADPOL	ADPOLEN	ADSD	ADSDEN

DACPOLEN Enable DACPOL. When this bit is set the DACPOL setting is output to the DAC circuit.

DACPOL DAC polarity setting; 0 = unipolar mode; 1 = bipolar mode.

ADPOL Unipolar output setting; 0 = bipolar mode; 1 = unipolar mode.

ADPOLEN Enable ADPOL. When this bit is set the ADPOL setting is output to the DAC circuit.

ADSD Single-ended/differential mode setting; 0 = differential mode; 1 = single ended mode.

ADSDEN Enable ADSD. When this bit is set the ADSD setting is output to the DAC circuit.

Page 2 Select Read Back Check: Base+15 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	PG2ID							

PGID Register page 2 ID. This register always contains the value 0xA2.

13. ANALOG-TO-DIGITAL INPUT RANGES AND RESOLUTION

13.1 Overview

Athena III uses a 16-bit A/D converter. The full range of numerical values for a 16-bit number is 0 - 65535. However, the A/D converter uses two's complement notation, so the A/D value is interpreted as a signed integer, ranging from –32768 to +32767.

The smallest change in input voltage that can be detected is 1/(216), or 1/65536, of the full-scale input range. This smallest change results in an increase or decrease of 1 in the A/D code, and is referred to as 1 LSB (1 Least Significant Bit).

The analog inputs on Athena III have three configuration options.

- Single-ended or differential mode
- Unipolar or bipolar mode
- Input range (gain)

The single-ended/differential and unipolar/bipolar modes are configured using jumper block J26, and apply to all inputs. The input range selection is done in software.

13.1.1 Input Range Selection

You can select a gain setting for the inputs, which causes them to be amplified before they reach the A/D converter. The gain setting is controlled in software, which allows it to be changed on a channel-by-channel basis. In general, you should select the highest gain (smallest input range) that allows the A/D converter to read the full range of voltages over which the input signals will vary. However, a gain that is too high causes the A/D converter to clip at either the high end or low end, and you will not be able to read the full range of voltages on your input signals.

13.1.2 Input Range Table

The table below indicates the analog input range for each possible configuration. The polarity is set using jumper block J26, and the gain is set with the G1 and G0 bits in the register at Base+3. The Gain value in the table is provided for clarity. Note that the single-ended vs. differential setting has no impact on the input range or the resolution.

Polarity	*G1*	*G0*	*Input Range*	*Resolution 1LSB*
Bipolar	0	0	±10V	305µV
Bipolar	0	1	±5V	153µV
Bipolar	1	0	±2.5V	76µV
Bipolar	1	1	±1.25V	38µV
Unipolar	0	0	Invalid	Invalid
Unipolar	0	1	0 - 10V	153µV
Unipolar	1	0	0 - 5V	76µV
Unipolar	1	1	0 - 2.5V	38µV

14. PERFORMING AN A/D CONVERSION

14.1 Introduction

This chapter describes the steps involved in performing an A/D conversion on a selected input channel using direct programming (without the driver software). Perform an A/D conversion according to the following steps. Each step is discussed in detail, below.

5. Select the input channel.
6. Select the input range.
7. Wait for analog input circuit to settle.
8. Initiate an A/D conversion.
9. Wait for the conversion to finish.
10. Read the data from the board.
11. Convert the numerical data to a meaningful value.

14.2 Select the Input Channel

To select the input channel to read, write a low-channel/high-channel pair to the channel register at Base+2. The low four bits select the low channel, and the high four bits select the high channel. When you write any value to this register, the current A/D channel is set to the low channel.

For example, to set the board to channel 4 only, write 0x44 to Base+2). To set the board to read channels 0 through 15, write 0xF0 to Base+2.

When you perform an A/D conversion, the current channel automatically increments to the next channel in the selected range. Therefore, to perform A/D conversions on a group of consecutively-numbered channels, you do not need to write the input channel prior to each conversion. For example, to read from channels 0 - 2, write 0x20 to base+2. The first conversion is on channel 0, the second will be on channel 1 and the third will be on channel 2. The channel counter wraps around to the beginning so the fourth conversion will be on channel 0, again.

If you are sampling the same channel repeatedly, set both high and low to the same value as in the first example, above. On subsequent conversions, you do not need to set the channel again.

14.3 Select the Input Range

Select the input range from among the available ranges. If the range is the same as for the previous A/D conversion it does not need to be set again. Write this value to the input range register at Base+3.

For example, for ±5V range (gain of 2), write 0x01 to Base+3.

14.4 Wait for Analog Input Circuit to Settle

After writing to the channel register, Base+2, or the input range register, Base+3, allow time for the analog input circuit to settle before starting an A/D conversion. The board has a built-in 10µS timer to assist with the wait period. Monitor the WAIT bit at Base+3, bit 5. When the bit value is 1, the circuit is actively settling on the input signal. When the value is 0, the board is ready to perform A/D conversions.

14.5 Perform an A/D Conversion on the Current Channel

After the above steps are completed, start the A/D conversion by writing to Base+0. This write operation only triggers the A/D if AINTE = 0 (interrupts are disabled). When AINTE = 1, the A/D can only be triggered by the on-board counter/timer or an external signal. This protects against accidental triggering by software during a long-running interrupt-based acquisition process.

```
outp(base,0x80);
```

14.6 Wait for the Conversion to Finish

The A/D converter chip takes up to five microseconds to complete one A/D conversion. Most processors and software can operate fast enough so that if you try to read the A/D converter immediately after starting the conversion, the read will occur faster than the A/D conversion and return invalid data. Therefore, the A/D converter provides a status signal to indicate whether it is busy or idle. This bit can be read back from the status register at Base+3, bit 7. When the A/D converter is busy (performing an A/D conversion), the bit value is 1 and the program must wait. When the A/D converter is idle (conversion is done and data is available), this bit value is 0 and the program may read the data.

The following statement is a simple example of this operation.

```
while (inp(base+3) & 0x80);  // Wait for conversion to finish before proceeding
```

The above example could hang your program if there is a hardware fault and the bit is stuck at 1. A better solution is to use a loop with a timeout, as shown below.

```
int checkstatus()    // returns 0 if ok, -1 if error
int i;
for (i = 0; i < 10000; i++)
{
       if !(inp(base+3) & 0x80) then return(0);       // conversion completed
}
return(-1);                                           // conversion did not complete
```

14.7 Read the Data from the Board

Once the conversion is complete, you can read the data back from the A/D converter. The data is a 16-bit value and is read back in two 8-bit bytes. The LSB must be read from the board before the MSB because the data is inserted into the board's FIFO in that order. Unlike other registers on the board, the A/D data may only be read one time, because each time a byte is read from the FIFO the internal FIFO pointer advances and that byte is no longer available. Reading data from an empty FIFO returns unpredictable results.

The following pseudo-code illustrates how to read and construct the 16-bit A/D value.

```
LSB = inp(base);
MSB = inp(base+1);
Data = MSB * 256 + LSB;   // combine the 2 bytes into a 16-bit value
```

The final data are interpreted as a 16-bit signed integer in the range -32768 to +32767.

> **Note:** The data range always includes both positive and negative values, even if the board is set to a unipolar input range. The data must now be converted to volts or other engineering units by using a conversion formula, as discussed below.

In scan mode, the behavior is the same except when the program initiates a conversion, all channels in the programmed channel range will be sampled once and the data will be stored in the FIFO. The FIFO depth register increments by the scan size. When STS goes low, the program should read out the data for all channels.

14.8 Convert the numerical data to a meaningful value

Once the A/D value is read, it needs to be converted to a meaningful value. The first step is to convert it back to the actual measured voltage. Afterwards, you may need to convert the voltage to some other engineering units. For example, the voltage may come from a temperature sensor and the voltage would then need to be converted to the corresponding temperature, according to the temperature sensor's characteristics.

Since there are a large number of possible input devices, this secondary step is not included here. Only conversion to input voltage is described. However, you can combine both transformations into a single formula if desired.

To convert the A/D value to the corresponding input voltage, use the following formulas.

14.8.1 Conversion Formula for Bipolar Input Ranges

Input voltage = A/D value / 32768 * Full-scale input range

Example:

Given, Input range is ±5V and A/D value is 17761.

Therefore,

Input voltage = 17761 / 32768 * 5V = 2.710V.

For a bipolar input range,

1 LSB = 1/32768 * Full-scale voltage.

The table, below, shows the relationship between A/D code and input voltage for a bipolar input range (VFS = Full scale input voltage).

A/D Code	*Input Voltage Symbolic Formula*	*Input Voltage for ±5V Range*
-32768	$-V_{FS}$	-5.0000V
-32767	$-V_{FS}$ + 1 LSB	-4.9998V
...	...	...
-1	-1 LSB	-0.00015V
0	0	0.0000V
1	+1 LSB	0.00015V
...	...	...
32767	V_{FS} - 1 LSB	4.9998V

14.8.2 Conversion Formula for Unipolar Input Ranges

Input voltage = (A/D value + 32768) / 65536 * Full-scale input range

Example:

Given, Input range is 0-5V and A/D value is 17761.

Therefore,

Input voltage = (17761 + 32768) / 65536 * 5V = 3.855V.

For a unipolar input range, 1 LSB = 1/65536 * Full-scale voltage.

The following table illustrates the relationship between A/D code and input voltage for a unipolar input range (VFS = Full scale input voltage).

A/D Code	*Input Voltage Symbolic Formula*	*Input Voltage for 0–5V Range*
-32768	0V	0.0000V
-32767	1 LSB (V_{FS} / 65536)	0.000076V
...	...	...
-1	V_{FS} / 2 - 1 LSB	2.4999V
0	V_{FS} / 2	2.5000V
1	V_{FS} / 2 + 1 LSB	2.5001V
...	...	...
32767	V_{FS} - 1 LSB	4.9999V

15. A/D SCAN, INTERRUPT AND FIFO OPERATION

The control bits SCANEN (scan enable) and AINTE (A/D interrupt enable) in conjunction with the FIFO determine the behavior of the board during A/D conversions and interrupts.

At the end of an AD conversion, the 16-bit A/D data is latched into the 8-bit FIFO in an interleaved fashion: first LSB, then MSB. A/D Data is read out of the FIFO with 2 read operations, first Base + 0 (LSB) and then Base + 1 (MSB).

When SCANEN = 1, each time an A/D trigger occurs, the board will perform an A/D conversion on all channels in the channel range programmed in Base + 2. When SCANEN = 0, each time an A/D trigger occurs, the board will perform a single A/D conversion and then advance to the next channel and wait for the next trigger.

During interrupt operation (AINTE = 1), the FIFO will fill up with data until it reaches the threshold programmed in the FIFO threshold register, and then the interrupt request will occur. If AINTE = 0, the FIFO threshold is ignored and the FIFO continues to fill up.

If the FIFO reaches its limit of 48 samples, then the next time an A/D conversion occurs the Overflow flag OVF will be set. In this case the FIFO will not accept any more data, and its contents will be preserved and may be read out. In order to clear the overflow condition, the program must reset the FIFO by writing to the FIFORST bit in Base + 1, or a hardware reset must occur.

In Scan mode (SCANEN = 1), the FIFO threshold should be set to a number at least equal to the scan size and in all cases equal to an integral number of scans. For example if the scan size is 8 channels, the FIFO threshold should be set to 8, 16, 24, 32, 40, or 48, but not less than 8. This way the interrupt will occur at the end of the scan, and the interrupt routine can read in a complete scan or set of scans each time it runs.

In non-scan mode (SCANEN = 0), the FIFO threshold should be set to a level that minimizes the interrupt rate but leaves enough time for the interrupt routine to respond before the next A/D conversion occurs. Remember that no data is available until the interrupt occurs, so if the rate is slow the delay to receive A/D data may be long. Therefore for slow sample rates the FIFO threshold should be small. If the sample rate is high, the FIFO threshold should be high to reduce the interrupt rate. However remember that the remaining space in the FIFO determines the time the interrupt routine has to respond to the interrupt request. If the FIFO threshold is too high, the FIFO may overflow before the interrupt routine responds. A good rule of thumb is to limit the interrupt rate to no more than 1,000-2,000 per second in Windows and Linux or 10,000 per second in DOS. Experimentation may be necessary to determine the optimum FIFO threshold for each application.

The table on the next page describes the board's behavior for each of the 4 possible cases of AINTE and SCANEN. The given interrupt software behavior describes the operation of the Diamond Systems Universal Driver software. If you write your own software or interrupt routine you should conform to the described behavior for optimum results.

The following table describes the register settings for the A/D operating modes. (LOW and HIGH channels referenced in the table are the 4-bit channel numbers in Base+2.)

AINTE Base+4, bit 0	*SCANE Base+2, bit 1*	*Operation*
0	0	Single A/D conversions are triggered by write to B+0. STS stays high during the A/D conversion. No interrupt occurs. The user program monitors STS (Base+3, bit 7) and reads A/D data when STS goes low.
0	1	A/D scans are triggered by write to B+0. All channels between LOW and HIGH are sampled. STS stays high during the entire scan (multiple A/D conversions). No interrupt occurs. The user program monitors STS (Base+3, bit 7) and reads A/D data when STS goes low.
1	0	Single A/D conversions are triggered by the source selected with ADCLK (Base+4, bit 4). STS stays high during the A/D conversion. A/D interrupt occurs when the FIFO reaches its programmed threshold. The interrupt routine reads the number of samples equal to the FIFO threshold (Base+5, bits 0-5).
1	1	A/D scans are triggered by the source selected with ADCLK (Base+4, bit 4). STS stays high during the entire scan (multiple A/D conversions). A/D interrupt occurs when the FIFO reaches its programmed threshold. The interrupt routine reads the number of samples equal to the FIFO threshold (Base+5, bits 0-5).

16. DIGITAL-TO-ANALOG OUTPUT RANGES AND RESOLUTION

16.1 Description

Athena III uses a 4-channel 12-bit D/A converter (DAC) to provide four analog outputs. A 12-bit DAC can generate output voltages with the precision of a 12-bit binary number. The maximum value of a 12-bit binary number is 2^{12} - 1, or 4095, so the full range of numerical values that the DACs support is 0 - 4095. The value 0 always corresponds to the lowest voltage in the output range, and the value 4095 always corresponds to the highest voltage minus 1 LSB. The theoretical top end of the range corresponds to an output code of 4096 which is impossible to achieve.

> **Note:** In this manual, the terms analog output, D/A, and DAC are all used interchangeably to mean the conversion of digital data originating from the Athena III computer hardware to an analog signal terminating at an external source.

16.2 Resolution

The resolution is the smallest possible change in output voltage. For a 12-bit DAC the resolution is $1/(2^{12})$, or 1/4096, of the full-scale output range. This smallest change results from an increase or decrease of 1 in the D/A code, so this change is referred to as 1 least significant bit (1 LSB). The value of this LSB is calculated as follows.

1 LSB = Output voltage range / 4096

Example:

For, Output range = 0-10V,

Output voltage range = 10V – 0V = 10V

Therefore,

1 LSB = 10V / 4096 = 2.44mV

Example:

For, Output range = ±10V;

Output voltage range = 10V – (-10V) = 20V

Therefore,

1 LSB = 20V / 4096 = 4.88mV

16.3 Output Range Selection

Jumper block J26 is used to select the DAC output range. The DACs can be configured for 0-10V or ±10V.

Two parameters are configured:

- unipolar/bipolar mode
- power-up/reset clear mode.

In most cases, for unipolar mode configure the board to reset to zero scale, and for bipolar mode configure the board for reset to mid-scale. In each case, the DACs reset to 0V.

16.4 D/A Conversion Formulas and Tables

The formulas below explain how to convert between D/A codes and output voltages.

16.4.1 D/A Conversion Formulas for Unipolar Output Ranges

Output voltage = (D/A code / 4096) * Reference voltage

D/A code = (Output voltage / Reference voltage) * 4096

Example:

For,

Output range in unipolar mode = 0 – 10V,

and,

Full-scale range = 10V – 0V = 10V,

if,

Desired output voltage = 2.000V,

D/A code = 2.000V / 10V * 4096 = 819.2 => 819

Note: the output code is always an integer.

For the unipolar output range 0-10V, 1 LSB = 1/4096 * 10V = 2.44mV.

The following table illustrates the relationship between D/A code and output voltage for a unipolar output range (VREF = Reference voltage).

D/A Code	*Output Voltage Symbolic Formula*	*Output Voltage for 0-10V Range*
0	0V	0.0000V
1	1 LSB (V_{REF} / 4096)	0.0024V
...	...	...
2047	V_{REF} / 2 - 1 LSB	4.9976V
2048	V_{REF} / 2	5.0000V
2049	V_{REF} / 2 + 1 LSB	5.0024V
...	...	...
4095	V_{REF} - 1 LSB	9.9976V

16.4.2 D/A Conversion Formulas for Bipolar Output Ranges

Output voltage = ((D/A code – 2048) / 2048) * Output reference

D/A code = (Output voltage / Output reference) * 2048 + 2048

Example:

For,

Output range in bipolar mode = ±10V

and,

Full-scale range = 10V – (-10V) = 20V

if,

Desired output voltage = 2.000V

D/A code = 2V / 10V * 2048 + 2048 = 2457.6 => 2458

For the bipolar output range ±10V, 1 LSB = 1/4096 * 20V, or 4.88mV.

The following table illustrates the relationship between D/A code and output voltage for a bipolar output range (VREF = Reference voltage).

D/A Code	*Output Voltage Symbolic Formula*	*Output Voltage for ±10V Range*
0	$-V_{REF}$	-10.0000V
1	V_{REF} + 1 LSB	-9.9951V
...	...	...
2047	-1 LSB	-0.0049V
2048	0	0.0000V
2049	+1 LSB	0.0049V
...	...	...
4095	V_{REF} - 1 LSB	9.9951V

17. GENERATING AN ANALOG OUTPUT

There are three steps involved in performing a D/A conversion, or generating an analog output. Each step is described in more detail, below. The descriptions use direct programming instead of driver software.

Compute the D/A code for the desired output voltage.

12. Write the value to the selected output channel.
13. Wait for the D/A to update.

17.1 Compute the D/A Code for the Desired Output Voltage

Use the formulas in the preceding section to compute the D/A code required to generate the desired voltage.

> **Note:** The DAC cannot generate the actual full-scale reference voltage; to do so would require an output code of 4096, which is not possible with a 12-bit number. The maximum output value is 4095. Therefore, the maximum possible output voltage is always 1 LSB less than the full-scale reference voltage.

17.2 Write the Value to the Selected Output Channel Registers

Use the following formulas to compute the LSB and MSB values.

LSB = D/A Code & 255 ;keep only the low 8 bits

MSB = int(D/A code / 256) ;strip off low 8 bits, keep 4 high bits

Example:

For,

Output code = 1776

Compute,

LSB = 1776 & 255 = 240 (0xF0)

and

MSB = int(1776 / 256) = int(6.9375) = 6

The LSB is an 8-bit number in the range 0-255. The MSB is a 4-bit number in the range 0-15.

The MSB is always rounded down. The truncated portion is accounted for by the LSB.

Write these values to the selected channel. The LSB is written to Base+6. The MSB and channel number are written to Base+7 (MSB = bits 0-3, channel number,0-3 = bits 6-7).

```
outp(Base+6, LSB);
outp(Base+7, MSB + channel << 6);
```

17.3 Wait for the D/A to Update

Writing the MSB and channel number to Base+7 starts the D/A update process for the selected channel. The update process requires approximately 30 microseconds to transmit the data serially to the D/A chip and update the D/A circuit in the chip. During this period, no attempt should be made to write to any other channel in the D/A through addresses Base+6 or Base+7.

The status bit DACBUSY (Base+3, bit 4) indicates if the D/A is busy updating (1) or idle (0). After writing to the D/A, monitor DACBUSY until it is zero before continuing with the next D/A operation.

18. ANALOG CIRCUIT CALIBRATION

The Athena III data acquisition circuit contains an advanced autocalibration circuit that can maintain the accuracy of both A/D and D/A circuits to within the specified tolerances regardless of time and temperature. Autocalibration is supported in the Diamond Systems Universal Driver software included with the board.

The autocalibration circuit uses an ultra-stable +5V reference voltage IC as the source for its calibration. Both A/D and D/A circuits are calibrated in the analog domain by using a series of 8-bit "TrimDACs" to adjust the offset and gain settings of the circuits. The data values driving the DACs are stored in an EEPROM and are loaded automatically each time the board powers up.

During the autocalibration process, the board will measure the on-board reference and calibrate the A/D circuit by adjusting the TrimDACs to achieve the best accuracy. Once the A/D circuit is calibrated, the D/A circuit is calibrated by routing the D/A outputs into the A/D converter and adjusting them as well. The new calibration values for the TrimDACs are stored back into the EEPROM so they can be automatically recalled thereafter.

A unique feature of Diamond's autocalibration process is that each analog input range is individually calibrated for optimum performance. Analog amplifier circuits with 16-bit accuracy exhibit gain and offset errors that vary depending on the gain setting. The settings that work best for one range may not be sufficient to calibrate another. If a circuit is calibrated for maximum accuracy in a particular input range, such as +/-5V, changing the input range to +/-10V or 0-2.5V may introduce errors that exceed the resolution of a 16-bit measurement and will require calibration again.

To counteract this phenomenon, Diamond's autocalibration circuit provides for a separate complete set of calibration settings for each analog input range. During the autocalibration process, each range is calibrated one at a time, and its set of calibration settings is stored in a separate area of the EEPROM's memory. One of these ranges is identified as the "boot range", and this range's calibration values are the ones that are automatically recalled during power-up. You have the option of specifying the boot range, which should be chosen as the range most commonly used in your application. When you change the input range, you have the option of loading the calibration values for the new input range to maintain optimum accuracy of your measurements.

The autocalibration process is triggered with a single function call in the Diamond Universal Driver software. The process takes about 10-20 seconds to calibrate the complete set of analog input ranges and about the same time for the D/A circuit. Autocalibration can easily be incorporated into your application program, so that you can calibrate the data acquisition circuit as often as necessary while your system is running.

19. DIGITAL I/O OPERATION

Athena III contains 24 digital I/O lines organized as three 8-bit I/O ports: Port A, Port B, and Port C. The direction of each port is programmable, and port C is further divided into two 4-bit halves, each with independent direction. The port data are accessed at registers Base+8 through Base+10, and the port direction register is located at Base+11.

Base +	***7***	***6***	***5***	***4***	***3***	***2***	***1***	***0***
8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
9	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
10	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
11	DIOCTR	-	-	DIRA	DIRCH	-	DIRB	DIRCL

The digital I/O lines are located at pins 1 through 24 on the I/O header J14. The lines are 3.3V and 5V logic compatible. Each output is capable of supplying –8mA in logic 1 state and +12mA in logic 0 state.

DIRA, DIRB, DIRCH, and DIRCL control the direction of ports A, B, C4-7 and C0-3. A direction value of 0 means output and 1 means input. All ports power up to input mode and the output registers are cleared to zero. When a port direction is changed to output, its output register is cleared to zero. When a port is in output mode, its value can be read back.

DIOCTR is used to control the function of lines C7-C4 on the I/O connector. When DIOCTR = 1, the lines are port C7-C4. When DIOCTR = 0, the lines are used for the counter/timer.

Pin No.	***DIOCTR = 1***	***DIOCTR = 0***	***Pin direction for DIOCTR = 0***
21	C4	Gate0	Input
22	C5	Gate1	Input
23	C6	Clk1	Input
24	C7	Out0	Output

20. COUNTER/TIMER OPERATION

Athena III contains two counter/timers that provide various timing functions on the board for A/D timing and user functions. These counters are controlled with registers in the on-board data acquisition controller FPGA.

20.1 Counter 0 – A/D Sample Control

Counter 0 is a 24-bit, "divide-by-n" counter used for controlling A/D sampling. The counter has a clock input, a gate input, and an output. The input is a 10MHz or 1MHz clock provided on the board and selected with bit CKFRQ0 in register Base+4, bit 5. The gate is an optional signal that can be input on pin 21 of I/O header J23 when DIOCTR (Base+11, bit 7) is 0. If this signal is not used, the counter runs freely. The output is a positive pulse whose frequency is equal to the input clock divided by the 24-bit divisor programmed into the counter. The output appears on pin 24 of the I/O header when DIOCTR is 0.

The counter operates by counting down from the programmed divisor value. When the counter reaches zero, it outputs a positive-going pulse equal to one input clock period (100ns or 1µs, depending on the input clock selected by CKFRQ0). The counter then reloads to the initial load value and repeats the process, indefinitely.

The output frequency can range from 5MHz (10MHz clock, divisor = 2) to 0.06Hz (1MHz clock divided by 16,777,215, or 224-1). The output is fed into the A/D timing circuit and can be selected to trigger A/D conversions when Base+4 register bits AINTE is 1 and ADCLK is 0. Using the control register at Base+15, the counter can be loaded, cleared, enabled and disabled. The optional gate can be enabled and disabled and the counter value can be latched for reading.

20.2 Counter 1 – Counting/Totalizing Functions

Counter 1 is similar to Counter 0 except that it is a 16-bit counter. Counter 1 also has an input, a gate and an output. These signals may be user-provided on the I/O header when DIOCTR is 0, or the input may come from the on-board clock generator. When the on-board clock generator is used, the clock frequency is either 10MHz or 100KHz, as determined by control Base+4 register bit CKFRQ1.

The output is a positive-going pulse that appears on pin 26 of the I/O header. The output pulse occurs when the counter reaches zero. When the counter reaches zero, it reloads and restarts on the next clock pulse. The output stays high for the entire time the counter is at zero; i.e., from the input pulse that causes the counter to reach zero until the input pulse that causes the counter to reload.

When DIOCTR is 0, Counter 1 operates as follows.

- It counts positive edges of the signal on pin 23 on the I/O header.
- The gate is provided on pin 22. If the signal is high, the counter counts. If the signal is low, the counter holds its value and ignores input pulses. This pin has a pull-up so the counter can operate without any external gate signal.

  NOTE: When counting external pulses, Counter 1 only updates its read register every fourth pulse. This behavior is due to the synchronous design of the counter having to contend with the asynchronous input pulses. The count register contents are correct on the fourth pulse but remain static until four additional pulses occur on the input.

When DIOCTR is 1, Counter 1 operates as follows.

The counter takes its input from the on-board clock generator based on the value of the Base+4 register CKFRQ1 bit. There is no gating and the counter runs continuously.

Counter 1 may be used as either a pulse generator or a totalizer/counter. In pulse generator mode, the output signal on pin 26 is of interest. In totalizer/counter mode, the counter value is of interest and may be read by first latching the value and then reading it. The width of the pulse is equal to the time period of the selected counters clock source.

20.3 Command Sequences

Diamond Systems provides driver software to control the counter/timers on Athena III. The information in this section is intended as a guide for programmers writing their own code, instead of using the driver, and to give a better understanding of the counter/timer operation.

The counter control register is located at I/O address base+15.

20.3.1 Load and Enable (Run) a Counter Sequence

14. Write the data to the counter. For counter 0, three bytes are required to load a 24-bit value. For counter 1, two bytes are needed for a 16-bit value. The value is an unsigned integer.

    Break the load value into 3 bytes: low, middle, and high, (Two bytes for Counter 1) and write the bytes to the data registers in any sequence.

    Counter 0:
    ```
    outp(base+12,low);
    outp(base+13,middle);
    outp(base+14,high);
    ```
    Counter 1:
    ```
    outp(base+12,low);
    outp(base+13,high);
    ```

15. Load the counter.

    Counter 0:
    ```
    outp(base+15,0x02);
    ```
    Counter 1:
    ```
    outp(base+15,0x82);
    ```

16. Enable the gate if desired. The gating may be enabled or disabled at any time. When gating is disabled, the counter counts all incoming edges. When gating is enabled, if the gate is high the counter counts all incoming edges and, if the gate is low, the counter ignores incoming clock edges.

    Counter 0:
    ```
    outp(base+15,0x10);
    ```
    Counter 1:
    ```
    outp(base+15,0x90);
    ```

17. Enable the counter. A counter may be enabled or disabled at any time. If disabled, the counter ignores incoming clock edges.

    Counter 0:
    ```
    outp(base+15,0x04);
    ```
    Counter 1:
    ```
    outp(base+15,0x84);
    ```

20.3.2 Read a Counter Sequence

18. Latch the counter.

Counter 0:
```
outp(base+15,0x40);
```
Counter 1:
```
outp(base+15,0xC0);
```

19. Read the data.

    The value is returned in 3 bytes, low, middle, and high (2 bytes for counter 1).

Counter 0:
```
low=inp(base+12);
middle=inp(base+13);
high=inp(base+14);
```
Counter 1:
```
low=inp(base+12);
high=inp(base+13);
```

20. Assemble the bytes into the complete counter value.

Counter 0:
```
val = high * 2^16 + middle * 2^8 + low;
```
Counter 1:
```
val = high * 2^8 + low;
```

20.3.3 Disabling the Counter Gate Command

- Disabling the counter gate, as shown below, causes the counter to run continuously.

Counter 0:

```
outp(base+15,0x20);
```

Counter 1:

```
outp(base+15,0xA0);
```

20.3.4 Clearing a Counter Sequence

Clear a counter to restart an operation. Normally, a counter is only cleared after stopping (disabling) and reading the counter. If you clear a counter while it is enabled, it continues to count incoming pulses so the counter value may not remain at zero.

21. Stop (disable) the counter.

Counter 0:

```
outp(base+15,0x08);
```

Counter 1:

```
outp(base+15,0x88);
```

22. Read the data (optional).

    The value is returned in 3 bytes, low, middle, and high (2 bytes for counter 1).

Counter 0:

```
low=inp(base+12);
middle=inp(base+13);
high=inp(base+14);
```

Counter 1:

```
low=inp(base+12);
high=inp(base+13);
```

23. Clear the counter.

Counter 0:

```
outp(base+15,0x01);
```

Counter 1:

```
outp(base+15,0x81);
```

21. USB FLASHDISK MODULE

Athena III is designed to accommodate an optional solid-state USB flashdisk module. This module contains 1GB to 8GB of solid-state non-volatile memory that operates like an USB drive without requiring additional driver software support.

Model	*Capacity*
FDU-1G-XT	1GB
FDU-2G-XT	2GB
FDU-4G-XT	4GB
FDU-8G-XT	8GB

Flashdisk Module

21.1 Installing the Flashdisk Module

The flashdisk module installs directly on connector J14 and is held down with a spacer and two screws onto a mounting hole on the board.

22. BIOS OPTION LISTING

This section describes the steps for modifying the BIOS settings and describes the BIOS screens.

22.1 Viewing and Modifying the BIOS Settings

During board startup, press function key <F2> to enter BIOS setup mode.

The main page displays the following menu options:

- Main
- Advanced
- GPIO Wake Configuration
- Chipset
- Boot
- Security
- Save & Exit

Select the menu option to view or modify the BIOS settings for the desired configuration area. The screens displayed for each area are described, below.

The following keyboard controls are available on any page for navigating the screen, as displayed at the bottom of each page.

Key	***Function***
F1	Help
Esc	Exit current screen
up-/down-arrow	Select setup item
left-/right-arrow	Select menu item
plus/minus symbols (+/-)	Change values
Enter	Execute command
F9	Save default values
F10	Save changes and exit BIOS setup mode

At any time, select Save & Exit to exit BIOS setup mode. Use the up/down arrow keys, followed by carriage return, to apply one of the exit actions.

22.2 BIOS Screen Descriptions

This section describes the screen displays for each BIOS setup area. The data in the fields are examples only and may be different depending on future product releases from Diamond Systems or the user's configuration. Sub-menus are prefixed with a ▶.

Main

BIOS Information	
BIOS Vendor	American Megatrends
Core Version	4.6.3.7
Project Version	0DATH 0.12
Build Date	09/07/2012 19:18:24
Product Name	Athena III
Motherboard Manufacturer	Diamond Systems
MRC Version	01.00
Total Memory	1024 MB (DDR2)
Platform Information	
System Language	[English]
System Date	[Fri 11/09/2012]
System Time	[23:00:26]
Access Level	Administrator

Advanced

Legacy OpROM Support	
Launch PXE OpROM	[Disabled]
Launch Storage OpROM	[Enabled]
▶ PCI Subsystem Settings	
▶ ACPI Settings	
▶ Windows CE	
▶ CPU Configuration	
▶ Wake On Lan Configuration	
▶ Thermal Configuration	
▶ USB Configuration	
▶ IO Ports Configuration	
▶ Hardware Health Monitor	
▶ Serial Port Console Redirection	

GPIO Wake Configuration

GPIO Wake Configuration	
Wake on GPIO0	[Disabled]
Wake on GPIO1	[Disabled]

Chipset

▶ North Bridge Chipset Configuration
▶ South Bridge Chipset Configuration
▶ IOH Configuration

Boot

Boot Configuration	
Quiet Boot	[Disabled]
Fast Boot	[Disabled]
Setup Prompt Timeout	1
Bootup NumLock State	[On]
CSM16 Module Version	07.65
GateA20 Active	[Upon Request]
Option ROM Messages	[Force BIOS]
Interrupt 19 Capture	[Disabled]
Boot Option Priorities	
Boot Option #1	[Disabled]

Security

Administrator Password
User Password

Save & Exit

Boot to Windows CE
Save Changes and Exit
Discard Changes and Exit
Save Changes and Reset
Discard Changes and Reset
Save Options
Save Changes
Discard Changes
Restore Defaults
Save as User Defaults
Restore as User Defaults
Boot Override
Built-in EFI Shell

23. SPECIFICATIONS

23.1 CPU

- Processor: Intel Atom E640T or E680T
- Speed: 1.0GHz or 1.6GHz
- Cooling: Heat sink with no fan
- Operating Temperature: -40ºC to +80ºC
- Chipset: Intel Topcliff I/O Hub
- SDRAM memory: 1GB 533MHz DDR2 soldered on-board
- Bus interface: PC/104 (ISA)
- Display type: VGA CRT and/or 24-bit dual channel LVDS flat panel
- VGA CRT resolution: 1600 x 1200 maximum
- LVDS flat panel resolution : 1280 x 768 maximum
- Video memory: 8/16/32MB shared with system memory
- USB ports: 4 USB 2.0
- Serial ports: 4 RS-232/422/485
    - Ports 1/2: Up to 115.2kbps, 16-byte FIFO, 16C450 compatible
    - Ports 3/4: Up to 460.8kbps, 128-byte FIFO, 16C2850 UART
- Networking: 1 10/100/1000Mbps Ethernet
- Mass storage interfaces: 1 SATA pin header
- USB flashdisk: solid state USB module supports up to 8GB and mounts to SBC
- Keyboard/mouse: PS/2
- Audio: AC ’97, Line-in, Line-Out, Mic

23.2 Data Acquisition Circuitry

- Analog inputs: 16 single-ended, 8 differential; user selectable
- A/D resolution: 16 bits
- Bipolar ranges: ±10V, ±5V, ±2.5V, ±1.25V
- Sample rate: 200KHz maximum total
- Unipolar ranges: 0-10V, 0-5V, 0-2.5V
- Input bias current: 100pA max
- Protection: ±35V on any analog input without damage
- Input Impedance: 10^13 ohms
- Relative accuracy: ±2 LSB after autocalibration
- Nonlinearity: ±3LSB, no missing codes
- Conversion rate: 100,000 samples/sec. max
- On-board FIFO: 2048 samples, programmable threshold
- A/D and D/A Calibration: Automatic using on-board microcontroller and temperature sensor
- Analog Outputs: 4, 12-bit resolution
- Output ranges: ±5V, ±10V, 0-5V, 0-10V
- Output current: ±5mA max per channel
- Settling time: 7µS max to 0.01%
- Relative accuracy: ±1 LSB
- Nonlinearity: ±1 LSB, monotonic

- Reset: Reset to zero-scale or mid-scale (jumper selectable)
- Waveform buffer: 1,024 samples
- Digital I/O lines: 24 programmable direction in 8-bit ports
- Input voltage: Logic 0: 0.0V min, 0.8V; max Logic 1: 2.0V min, 5.0V max
- Input current: ±1µA max
- Output voltage: Logic 0: 0.0V min, 0.33V; max Logic 1: 2.4V min, 5.0V max
- Output current: Logic 0: 12mA max per line Logic 1: -4mA max per line
- A/D Pacer clock: 24-bit down counter (source: 10MHz, 1MHz or external signal)
- General purpose: 16-bit down counter (source: 10MHz, 100KHz or external signal)

23.3 Power Supply

- Input Voltage: +5VDC ±5%
- Power consumption: 9.4W

23.4 General

- Shock: IEC68-2-27 compatible
- Vibration: MIL-STD-810E 514.4 compatible
- Dimensions: 4.18 x 4.48 in. (106 x 114mm)
- Weight: 8.8oz.(249g) with heat sink
- RoHS: Compliant